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FACULTAD DE INGENIERÍA

MEDIUM-VOLTAGE PHOTOVOLTAIC SYSTEMS BASED ON MULTILEVEL INVERTERS WITH ENERGY STORAGE SUPPORT

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Presented by

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Advisor:

Dr. Víctor Manuel Cárdenas Galindo

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Medium-Voltage Photovoltaic Systems Based on Multilevel Inverters with Energy Storage Support

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En atención a su solicitud de Temario, presentada por el **Dr. Víctor Manuel Cárdenas Galindo,** Asesor de la Tesis que desarrollará Usted con el objeto de obtener el Grado de **Doctor en Ingeniería Eléctrica**, me es grato comunicarle que en la sesión del H. Consejo Técnico Consultivo celebrada el día 16 de diciembre del presente año, fue aprobado el Temario propuesto:

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1. Introducción.
2. Sistemas fotovoltaicos y sistemas de almacenamiento de energía en baterías
3. Convertidor CD-CD para aplicaciones fotovoltaicas con almacenamiento de energía basado en el convertidor 3L
4. Análisis y diseño de un convertidor CD-CA-CA en cascada con enlace en CA
5. Conclusiones
   Anexos
   Referencias

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HACE CONSTAR

Que la tesis que tiene por título:

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Presentada por el Sr.

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Aclaración

El presente trabajo que lleva por título:

Medium-Voltage Photovoltaic Systems Based on Multilevel Inverters with Energy Storage Support

Se realizó en el periodo Septiembre de 2017 a Diciembre de 2022 bajo la dirección del Dr. Víctor Manuel Cárdenas Galindo.

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CV

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His research interests include power converters for renewable energy generation systems, converters with high-frequency links, multilevel converters, energy storage systems, control hardware in the loop systems, real-time simulators and control rapid prototyping tools.

ENGLISH SUMMARY

The use of renewable energies is one of the ways to fight global warming and try to limit the temperature increase to 1.5°C by 2050. Renewable energy technologies deployment has been increasing in the last ten years due to price reduction of materials, new developments, and government and policy initiatives. The uneven deployment has brought challenges in operating electric systems with a high share of variable renewable energies. The affected systems must be more flexible but also operate with reliability.

Photovoltaic (PV) solar energy has been one of the renewable energies with more growth due to the increase in efficiency and reduction of PV cell cost; this has led to the construction of Terawatt PV solar plants. For example, Bhadla Solar Park in India is a project with a capacity of 2.24 GW. Mega projects will continue to be installed around the world, and this will require new developments in power electronic converters, specifically in Medium Voltage (MV) applications where such huge PV plans are installed. Therefore, many investigations focus on developing and implanting new topologies to incorporate large-scale PV plants into the medium voltage grid. Some works have tried to implement converters based on the serial configuration of discrete switches to reach medium voltage levels; others are using multilevel topologies. Depending on the investigation line, there are problems to face, like isolation, volume reductions, voltage drifts, and partial shading, among others.

In this regard, the Ph.D. dissertation proposes a multilevel converter based on medium-frequency AC links that allow large-scale PV plants to be interfaced with the grid at medium voltage levels. The proposed converter is based on cascading three-phase DC-AC-AC converters. The cascading feature lets implement low-rated switched devices; additionally, it allows generating of different DC links in which separate maximum power point tracker (MPPT) plus control law strategies can handle partial shading among the PV plant. Overall above, the cascade feature makes the system modular, an attractive characteristic for large-scale systems.

Energy storage devices have the possibility to absorb, store and inject electricity into the grid. The most common mode to store energy is pumped hydro, which is the predominant technology around the globe to store energy [1]. It has demonstrated that it can shift energy for a long time and a vast amount of energy. However, there are other ways to store energy, and recently electrochemical has attracted the attention of many investigations. Batteries have evolved drastically; for example, lithium-ion batteries have reached high efficiency, specific energy, and specific power while dropping production costs. This is important because it opens new ways for a system operator based on PV installations to provide extended services to the grid.

On the other hand, storage can increase PV harvesting by reducing power curtailment at the mid-day when solar irradiance is high, storing and injecting surplus energy into the system later. Electricity storage will play an essential part in accelerating energy transition by allowing variable renewable energies to be integrated into the grid. On the previous subject, this Ph.D. work takes advantage of storage energy systems and implements them on the proposed structure. Before employing it, a review of the battery model and DC-DC bidirectional converters is done; later, charging and discharging strategies are analyzed.

This work proposes a complete power electronic converter for large-scale integration of photovoltaic systems plus energy storage to the medium-voltage grid. The proposed multilevel converter with energy storage is validated through simulations, some parts of the work are validated by control hardware in the loop simulations and other sections are validated on a scale-down laboratory prototype. Additionally, a control strategy for partial shading is discussed.

RESUMEN EN ESPAÑOL

El uso de energías renovables es una de las maneras en que se puede combatir el calentamiento global y a su vez intentar limitar a 1.5 °C el incremento de temperatura para el 2050. El esparcimiento de las tecnologías de energías renovables se ha incrementado en los últimos diez años debido a la reducción de los precios de las materias primas, nuevos desarrollos, y a las iniciativas y políticas gubernamentales. Este despliegue irregular ha traído retos en la operación de sistemas eléctricos que tienen una alta penetración de sistemas basados en energías renovables variables. Los sistemas afectados deben ser flexibles, pero también operar con fiabilidad.

La energía solar fotovoltaica (PV) ha sido una de las energías renovables con mayor crecimiento debido al incremento en la eficiencia y a la reducción de los costes de las celdas PV; esto ha conducido a la construcción de plantas solares PV de Terawatts de capacidad instalada. Por ejemplo, el parque solar Bhadla en India es un proyecto con una capacidad de 2.24 GW. Los megaproyectos continuarán instalándose alrededor del mundo, y esto requerirá nuevos desarrollos en lo que respecta a convertidores de electrónica de potencia, específicamente en aplicaciones en media tensión donde las inmensas plantas PV son conectadas. Por consiguiente, muchas investigaciones se han enfocado en el desarrollo e implementación de nuevas topologías para incorporar plantas fotovoltaicas de gran escala en la red de media tensión. Algunos trabajos han intentado implementar convertidores basados en la configuración en serie de múltiples interruptores discretos para alcanzar niveles de media tensión; mientras otros están usando topologías multinivel para alcanzar el mismo objetivo. Dependiendo de la línea de investigación, hay problemas a enfrentar como el aislamiento, la reducción de volumen, el desvíos de tensión y el nublado parcial, entre otros.

En este sentido, este trabajo de tesis doctoral propone un convertidor multinivel basado en enlaces de CA en media frecuencia que permitan a las plantas PV de gran escala interconectarse a la red en niveles de media tensión. El convertidor propuesto se conforma colocando en cascada convertidores trifásicos CD-CA-CA. La configuración en cascada permite usar interruptores de potencia de menores prestaciones; adicionalmente, también permite generar diferentes enlaces de CD, en los cuales algoritmos de seguimiento del máximo punto de potencia (MPPT) independientes, más las estrategias control, permiten operar la planta fotovoltaica a pesar del sombreado parcial. Sobre todo, la configuración en cascada permite que el sistema sea modular, una característica atractiva para sistemas de gran escala.

Los dispositivos de almacenamiento de energía tienen la posibilidad de absorber, almacenar e inyectar electricidad hacía la red. La forma más común de almacenar energía es a través de plantas hidráulicas de bombeo, la cual es la tecnología para almacenamiento de energía predominante alrededor del mundo. Este tipo de tecnología ha demostrado que puede intercambiar energía por largos periodos de

tiempo o por grandes cantidades de energía. Sin embargo, hay otras maneras de almacenar energía, y recientemente la energía electroquímica ha atraído la atención de muchas investigaciones. Las baterías han evolucionado drásticamente; especialmente las baterías de iones de litio que han alcanzado una alta eficiencia, energía y potencia específicas, mientras sus precios de producción disminuyen. Esto es importante ya que abre nuevas formas en como un operador de red basado en instalaciones fotovoltaicas puede proveer servicios extendidos a la red.

Por otro lado, el almacenamiento puede incrementar el aprovechamiento fotovoltaico mediante la reducción de recortes de potencia a mediodía cuando la irradiación solar es alta, entonces se almacena la energía que de otra forma no sería aprovechada, e inyectándola a la red en un mejor momento. El almacenamiento eléctrico jugará un papel esencial acelerando la transición energética, permitiendo a las energías renovables variables integrarse a la red. Por lo cual, este trabajo de doctorado toma las ventajas de los sistemas de almacenamiento y los implementa en el sistema propuesto. Antes de la implementación de estos, se lleva a cabo una revisión del modelo de la batería y de los convertidores DC-DC bidireccionales; después, se analizan estrategias de carga y descarga de baterías.

Este trabajo propone un convertidor de electrónica de potencia para la integración de sistemas fotovoltaicos de gran escala en la red de media tensión considerando sistemas de almacenamiento. El convertidor multinivel propuesto con almacenamiento de energía es validado a través de simulaciones en computadora, otras partes del trabajo son validadas en simuladores en tiempo real; mientras otras secciones del trabajo se probaron en un prototipo de laboratorio a escala reducida. Adicionalmente, se discuten estrategias de control para enfrentar los retos que el nublado parcial presenta.

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I had a great time in Mexico at the UASLP and Denmark at the AAU. I learned a lot from both institutions; there are differences between them and things in common, but, in both places, you can find people who want the best for our world.

Manuel Barrios.

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CHAPTER 1. INTRODUCTION

1.1. MOTIVATION

There is a challenge: try to reduce 45% of the earth's greenhouse gas emission from 2010 levels by 2030. Every day is more evident the need to accelerate the energy transition by means of the use of more renewable energy sources. Climate change is more palpable, and it can be seen in the increase in extreme weather conditions around the world. To face this, persuasive policy actions are taking place in different countries. These strategies are translated, for example, that the prices of renewable energy (RE) have fallen to the point that fossil-based energy is no longer desirable in some areas. As proof of this, according to the global weighted-average Levelized Cost of Energy (LCOE), the price for electricity from utility-scale photovoltaics (PV) plants has fallen 85% in the last decade from USD 0.381/kWh to USD 0.057/kWh [2]. Therefore, utility-scale solar PV energy can now contend against the cheapest new fossil-fuel energies like new coal-fired generation options [3]. This affordable energy is partially achieved thanks to the fall in prices of crystalline silicon solar PV modules in the last years. Figure 1.1 shows how the cost of thin-film a-Si/u-Si or Global Index has fallen in Europe from 2011 to 2021.

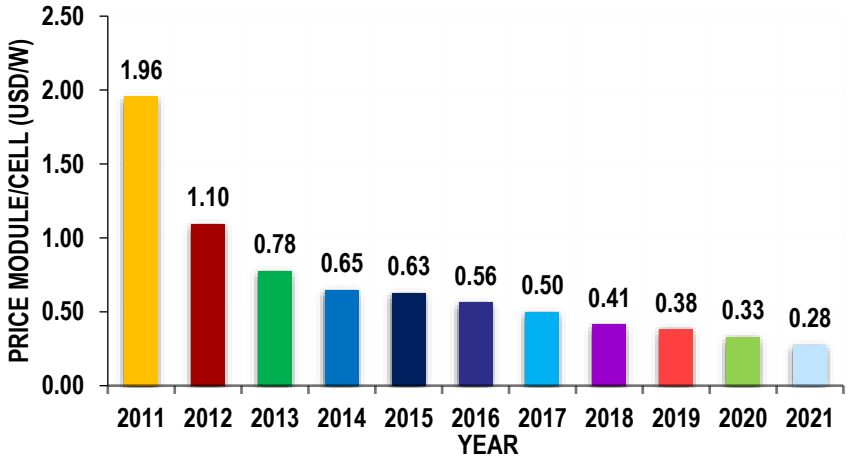

Figure 1.1: Module/Cell cost reduction.

In 2021, the global renewable generation capacity installed was 2802 GW. As seen in Figure 1.2, Hydropower energy is the most widespread renewable energy taking up 43% of the total. In the second place, Wind energy shares this place with Solar energy with 26% of the total global renewable generation capacity. Finally, the remaining 5% are from other renewable energies, including bioenergy (biofuels and renewable

waste, liquid biofuels) and Geothermal energy. Solar energy was the renewable energy with the most significant growth (see Figure 1.3), reaching a global capacity of 709.67 GW by the end of 2020 [4].

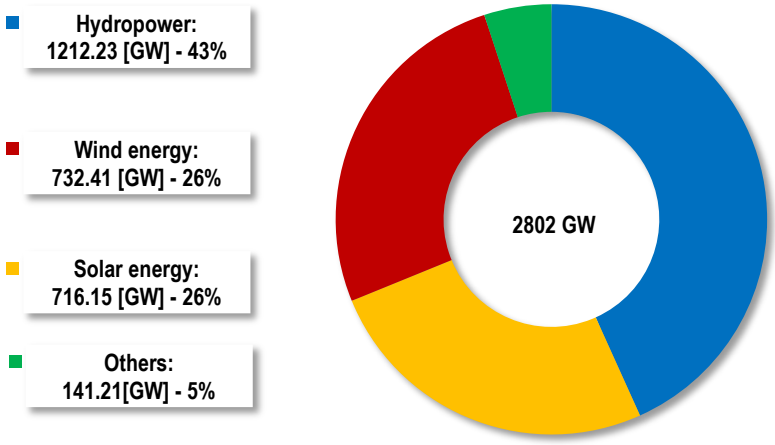

Figure 1.2: Renewable capacity energy 2021.

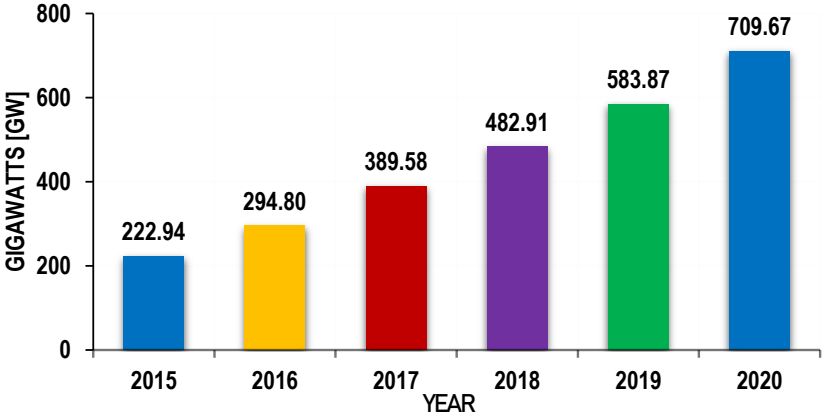

Figure 1.3: Cumulative installed PV solar energy capacity.

This massive deployment of Solar PV energy is mainly related to reducing module PV cost; here, manufacturers have optimized the process, reduced labor costs, and increased efficiency, which is also a key driver. The module efficiency of crystalline PV modules has risen from 14.7% in 2010 to 20% in 2020. Due to reduced PV cell costs and high government initiatives to stop fossil-based energy, hundreds of MW-level PV power plants are being constructed and connected to the grid annually[5-7]. It is expected that massive power plants will be installed over the following years. SolarPower Europe forecasts in the low scenario that by 2025 the global capacity for

PV solar energy will grow from 757 GW in 2021 to 1,553 GW. In the best-case scenario, the forecast estimates that the capacity would grow to 2,147 GW Figure 1.4.

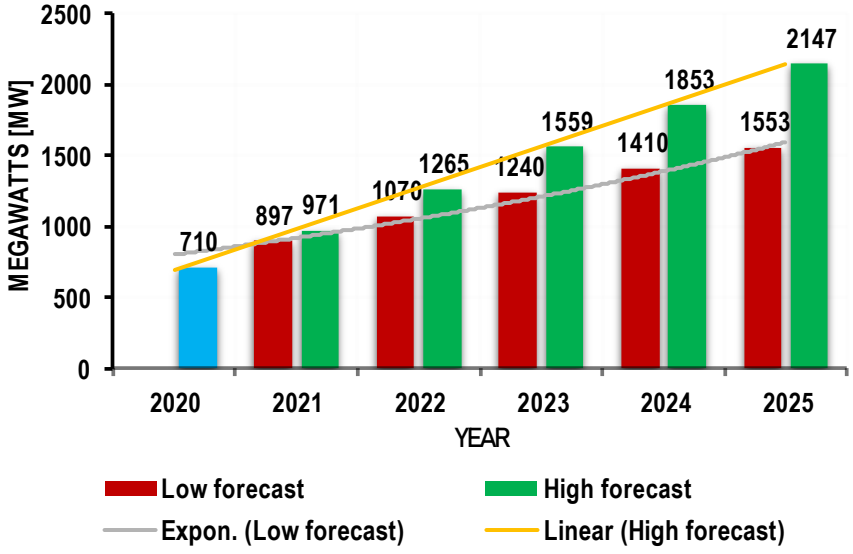

Figure 1.4: PV capacity forecast.

The installation of gigawatt PV power plants in the coming years will require new developments in the power electronic converter area. This power converter, from now on referred to as an inverter, needs to handle enormous quantities of power. It is required to convert the low voltage direct current (DC) to high voltage alternating current (AC), always taking into consideration that this conversion must be done efficiently. Because the PV plants will be connected to the utility, it will be necessary and required that the inverter perform extra tasks, not only the conversion of energy but also performing auxiliaries service to the grid. To provide additional auxiliary services to the grid, energy storage support is required; for example, to provide energy time-shifting (Figure 1.5), it is needed a storage unit that allows the capture of energy from the PV system during the daytime or during the high harvesting period, and then injects the energy at a different time, for instance at evening, to take advance when higher power purchase agreement (PPA) rates in peak periods or when there are high peak demands from the grid at what time there is no PV generation. The same procedure can be followed during partially cloudy periods; the energy storage system will allow the inverter to inject the same amount of power into the grid, leading the system to provide capacity firming to the utility.

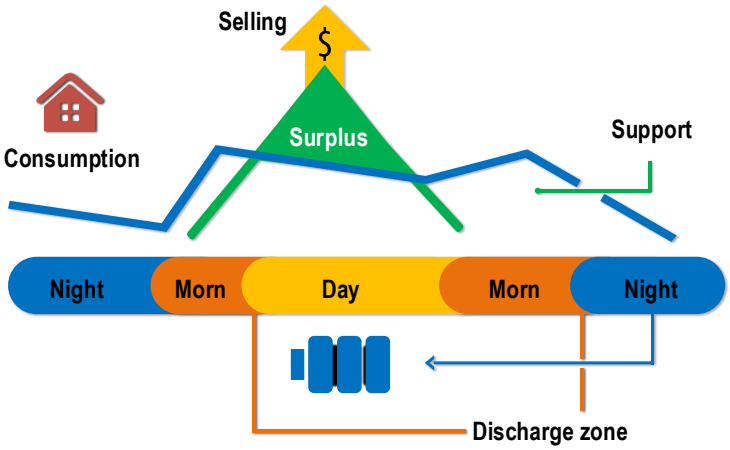

Figure 1.5: Energy time-shifting scheme.

In the past, storage system integration to the grid was considered nonprofitable because the system value of storage was poorly understood for electricity markets; in consequence, investors found storage projects inviable to produce revenues or complex to justify being built. Providing services such as energy time shifting, capacity firming, lowering curtailment, or reducing the needing to use peaking plants by means of electricity storage indirectly can produce cost reductions by participating in multiple markets (stacking revenues) to increase revenues and maximize profitability [1]. In this sense, multiple projects (section 2.2) around the world have implemented energy storage solutions to support the integration of large-scale penetration of RE into the grid and to increase revenues.

The Electricity Storage Valuation Framework [8], written by the International Renewable Energy Agency (IRENA), gives a detailed analysis of the economic suitability for installing energy storage into the grid. The study provides how to determine the benefits, conditions, and project viability to successfully incorporate battery energy storage into the grid. Additionally, real-world examples of cost-effective storage deployment are given. These examples show how to stack multiple revenue streams to reach commercial viability. Some policies and regulations are suggested to support cost-effective storage installations in cases where the project cost is higher than the project revenues due to unfavorable market conditions.

Battery storage will be an essential key to decarbonizing the electric system. Battery costs are going down due to the mass-production. For example, electric vehicle batteries in 2010 were USD 1100/kWh, but by 2020, these prices fell to USD 137/kWh [8]. In the case of utility-scale batteries (US) for the United States, the price was around USD 2252/kWh for 2015 and USD 589/kWh for 2019 [9]. Therefore, it is economically viable to provide and expand auxiliaries services due to cost reduction.

It is expected that the current battery production capacity (180 GWh) will increase to 3 TWh by 2030, thanks to the installation of a large number of GWh battery factories [10].

To supply ancillary services to the grid, it is necessary to install the US batteries at some point in the utility. Basically, there are two techniques to interconnect a US Battery Energy Storage System (BESS) to a Medium Voltage (MV) grid, AC-coupling and DC-coupling. The most widespread configuration [11] is depicted in Figure 1.6 (a); it is an AC-coupling structure, where an array of batteries are connected to a DC-DC converter to boost up the voltage; later, a converter transforms the DC-link voltage generated by the DC-DC converter to an AC voltage (DC-AC stage) that a line frequency (LF) transformer will isolate and step up to an MV utility level. There are alternatives where the DC-DC converter is not implemented.

Most of the commercial solutions for the DC-AC converter are based on two-level (2L) or three-level (3L) configurations [12-14]. However, there are other topologies called multilevel converters that are also being deployed for BESS applications, for example, Neutral Point Clamped (NPC), Active NPC, and Flying Capacitor (FC) [12, 15-17]. The advantage of multilevel inverters is that they allow to increase the output voltage and present a better harmonic performance. Moreover, transformerless alternatives, such as the Cascaded H-Bridge (CHB) or the Modular Multilevel Converter (MMC), present lower losses and outstanding modularity characteristics. In any case, AC-coupling has the disadvantage that it requires installing an additional inverter and step-up transformer, which increases the installation cost.

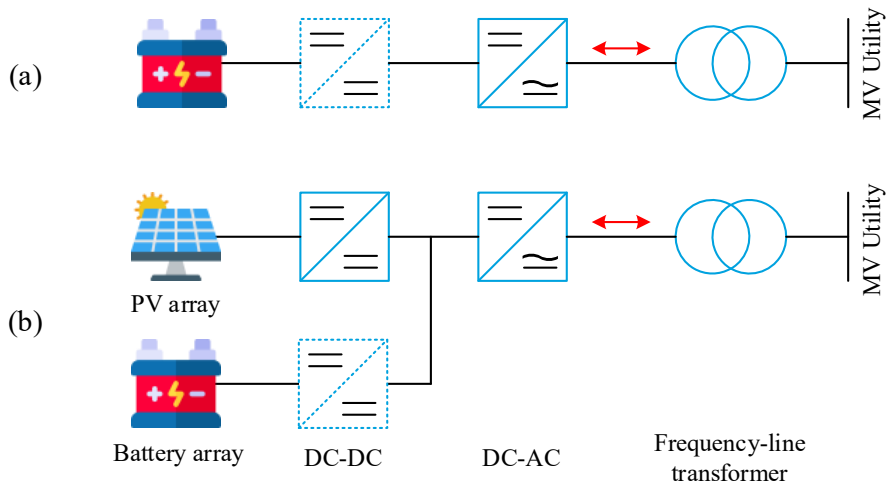

Figure 1.6: BESS coupling: (a) AC-coupling. (b) DC-coupling.

In contrast with the AC-coupling, DC-coupling (Figure 1.6 (b)) does not require the installation of an extra inverter and an LF transformer to add storage to a new or an already installed PV plant. DC-coupling configuration requires only a bidirectional DC-DC converter that is interfaced with the DC-link.

For the DC-DC converter, there are two options, non-isolated and isolated topologies. In the first case, the most widespread converters are the bidirectional buck-boost, cascaded, Cúk, SEPIC, interleaved, switched-capacitor, quadratic buck-boost, half-bridge, and multilevel converters. For the second case, some examples include the flyback, Zeta, push-pull, forward, dual active bridge (DAB), dual half-bridge, LLC resonant converter. The most common solutions of each case are the boost and the DAB topologies respectively [16].

The state-of-the-art utility-scale BESS considers DC-coupling systems accompanied by multilevel inverters with AC-link. This kind of system provides isolation between the grid and the BESS as well as the PV systems while keeping the transformer and the output filter small compared with the bulky LF transformer in traditional BESS for utility-scale PV power plants.

S. Essakiappan et al. propose in [18] a converter for intermittency mitigation in MV PV systems. The proposed converter is a multilevel inverter with a medium-frequency transformer link. The PV plant is divided into zones, and the DC voltage of each zone is transformed to an MF AC voltage that feeds the MF transformer with three secondary windings to feed a full bridge converter to generate a three-phase system. In that work, sodium–sulfur (NaS) battery solution is used for the BESS. The BESS is midpoint grounded as well as the PV system, reducing the bus-to-ground voltage. The batteries are interfaced to the PV system DC bus (DC-coupling) by a bidirectional DC-DC three-level buck-boost converter. This configuration allows the converter's switches to block half of the input voltage; therefore, low-voltage rate switches can be used. The battery charging and discharging operation modes are discussed in that work. Additionally, a 125 kW BESS simulation is provided. Finally, experimental results for a scaled-down laboratory prototype are given.

Wei Xu et al. present in [19] propose combining PV and BES into a single inverter system without the LF step-up transformer. In this proposal, the battery is connected to the DC link bus by a bidirectional boost converter, and the DC power can charge it from the PV or the grid; therefore, the proposal is a DC-coupled BESS. This proposal is based on a solid-state transformer (SST) for a 13.8 kV grid with a 1.5 kV PV farm. The SST implements a modular concept with 27 SiC submodules; a DC-AC DAB converter integrates each submodule with a modular architecture in which multiple low-voltage submodules are connected in series to reach MV levels. MF transformer is designed to obtain high efficiency while keeping the system isolated. The control architecture is focused on voltage balancing and real and reactive power.

Salwan Sabry and Prasad Enjeti proposed in [20] a high-frequency (HF) integrated solid-state transformer for the utility interface of solar PV plus BESS. Three AC-AC converters integrate the primary side of the transformer with a DC link connected to an HF transformer. The secondary side of the HF transformer is coupled to three-phase PWM current source converters (CSC). The input of the AC-AC converter is fed by 20 kHz AC square voltage. The CSC is controlled with selective harmonic elimination PWM technique. Simulation results consider a 120 kW solar PV system with 1.5 kV of DC input voltage. A scaled-down laboratory prototype is developed to verify the concept. The proposal converter presents a higher input power quality due to eliminating low-order harmonics. The absence of DC-link and electrolytic capacitors makes the CSC more robust.

To the extent that the use of renewable energies grows exponentially, and because the integration of energy storage systems is essential, the electric system requires more flexibility from the power plants. This flexibility can be achieved through new developments in the power electronics field, specifically in medium voltage converters with high power, high efficiency, and high-reliability features required to integrate to the grid massive large-scale PV systems that will be installed in the coming years. In this regard, this thesis work proposes a cascaded DC-AC-AC medium-voltage grid-tied power electronic converter for large-scale PV plants with energy storage support which diagram is shown in Figure 1.7.

The proposed power electronic converter is integrated by two stages, DC-DC and DC-AC, with a common DC-link. Two subsystems integrate the first stage; the PV and BESS subsystems which are coupled by DC-DC converters to the DC-link. The second stage consists of three-phase DC-AC-AC cascaded converters.

The first subsystem (blue DC-DC converter in Figure 1.7) is associated with the PV modules; these PVs are interconnected in a serial-parallel array to reach the voltage and power level required by the application and regulations. Then, the PV array is interconnected with a three-level bidirectional converter (3LBDC) which will extract the maximum power available in the PV array and boost the voltage to a proper DC-link level (1 kV for simulation proposes). The second subsystem (white DC-DC converter) comprises the BESS, which is integrated by a battery array and a 3LBDC converter. This subsystem, among other things, will step up the battery voltage (from 250 V) to the DC-link level and serve as a charger when the power flows come from the PV or the grid towards the battery. In the second stage (DC-AC), a three-phase (3PH) seven-level (7L) DC-AC-AC converter is implemented to interface the PV and BESS subsystems to the utility.

The operation of the proposed topology will be verified by means of simulations developed in PSIM, control hardware in the loop, from now on C-HIL, in Typhoon-HIL, and on a scale-down laboratory prototype.

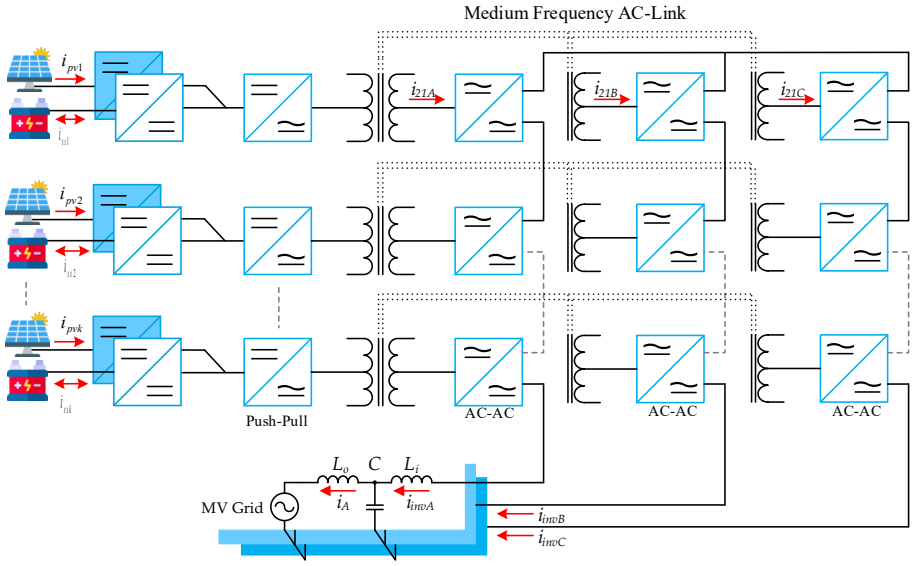

Figure 1.7: Proposed power electronic topology for this thesis work.

The entire topology simulation considers three cascaded converters: the output voltage, output power, and DC-link voltage are 13.20 kV (phase-to-phase), 324.16 kW (based on the PV plant), and 1 kV, respectively; more details are found in the chapter four. In the case of the C-HIL simulations, one stand-alone three-phase DC-AC-AC converter in a closed-loop is considered. The output voltage, output power, and DC-link are 400 V (phase-to-phase), 10 kW, and 650 V, respectively. Finally, in the case of the laboratory prototype, a similar configuration to the previous setup is taken into account; the difference is that this is a scale-down converter with an output voltage of 400/3 V, rated at 3 kW, with an input voltage of 120 V.

1.2. RESEARCH HYPOTHESIS AND QUESTIONS

1.2.1. HYPOTHESIS

It is possible to use DC-AC-AC cascaded converters based on MF-AC links with energy storage to inject power to the MV grid under partial shading over the different PV arrays while keeping the DC-link of every cascaded converter regulated and considering that there is a single global cascaded control loop.

1.2.2. RESEARCH QUESTIONS

As explained in the motivations, more investigation is needed to integrate large-scale renewable energy into the grid. To contribute to this area of study, the following research questions were formulated and answered during the development of this thesis.

- How to make the most of the proposed converter to interconnect large-scale PV systems to the MV grid?
- What are the possibilities for the proposed multilevel converter with large-scale photovoltaic systems if a battery energy storage system solution is considered?
- How to control multiple DC links of the proposed multilevel converter under a single cascaded loop control technique while regulating the injecting current?
- How to inject power into the grid under uneven irradiance circumstances while keeping the DC links regulated?
- How to avoid using a two-step conversion strategy for interconnecting the MF-AF voltage stage to the LF-AC voltage stage?
- How to reduce the inductor ripple on the DC-DC converter without increasing the inductor size?
- What kind of battery model is needed to probe battery charging and discharging technique while considering the effect of the battery voltage drop?

1.3. THESIS OBJECTIVES AND LIMITATIONS

To analyze and develop a grid-tied multilevel converter in medium voltage level for PV applications considering an energy storage solution that helps integrate large-scale PV energy into the grid.

1.3.1. SCOPES AND PARTICULAR OBJECTIVES

- To study and compare energy storage solutions for PV integration to the grid.

- To model the PV module and the battery.
- To propose a multilevel converter to integrate large-scale PV energy into the grid that can address the issues of previous research.
- To propose a converter that can integrate energy storage into the multilevel converter.
- To investigate a suitable control strategy to inject power into the grid under partial shading as well as develop control strategies to charge and discharge the BESS from the grid and the PV system and verify and test the proposed multilevel converter based on C-HIL simulation and experimental tests.

1.3.2. PROJECT LIMITATIONS

There are several considerations, assumptions, and limitations in this thesis work:

- Power electronic switches are considered ideal; thus, no parasitic components are taken into account.
- Efficiency stability and robust analysis are not developed for this work.
- The multilevel converter is connected to the grid by an LCL filter, where the second inductor is the grid impedance.
- The real-time simulator used in this work has a limited number of cores and topologies. The power electronic topology studied in this work is not part of Typhoon's library; therefore, it was developed from scratch. The developed model presents unexpected behaviors that this author or the manufacturer could not solve.
- The experimental prototype is limited to designing and validating one cascaded three-phase DC-AC-AC converter and operates in grid-forming mode.
- A cost evaluation or projection for designing a d building for the proposed solution was not evaluated, and this topic is out of the scope of this thesis work.

1.4. THESIS OUTLINE

Chapter 2 presents an introduction to PV modeling, PV plus series and shunt resistances model is selected for this work. PV topology is as well presented in this section and gives an overview of how PV arrays are connected. In order to harvest all the available power in the PV-arrays, maximum power point trackers are studied. Energy storage systems are reviewed and analyzed, in particular batteries. A generic mathematical model of a battery is studied to be implemented in this work. The advantages and disadvantages of storage with DC or AC coupling are presented. Finally, PV plus storage systems possibilities are briefly explored.

Chapter 3 presents a review of the most interesting bidirectional DC-DC converters for battery energy storage system applications, where the three-level bidirectional converter is chosen due to its convenient features for battery applications. Next, the operation principle is addressed, accompanied by the power electronics design, where the size of the inductor and flying capacitor are obtained. After the converter's design, the control scheme is analyzed, and the controller has to cope with the flying capacitor voltage regulation and the BESS charging and discharging process. Finally, a set of simulations are performed to verify the proper operation of the converter's control scheme. The simulations are the following: control strategy to charge a li-ion battery, three-level converter working as an MPPT tracker, and PV system plus BESS.

Chapter 4 studies the state-of-the-art of multilevel topologies focusing on topologies with medium-frequency AC-link with two and direct stage conversion. Then, the proposed converter is presented, its operating principle is explained, and the sizing of the converter is developed. Soon after, the inner loops are designed, and the control structure for the multilevel converter under partial shading conditions is described. This chapter also presents the results in three ways: software simulations developed in PSIM considering the full proposed converter, control hardware in the loop simulations (dSPACE with Typhoon-HIL platform), and open and closed-loop experimental results developed on scale-down laboratory prototypes where the converter's concept is proven.

Chapter 5 presents the conclusions of this work and introduces possible future outcomes.

1.5. LIST OF PUBLICATIONS

[1]. A. Sim, A. Houari, M. A. Barrios, M. A. Ahmed, M. Machmoum and J. M. Guerrero, “Power management strategy with SoCs balancing of a battery powered shipboard DC Microgrid,” Conférence Internationale en Sciences et Technologies Electriques au Maghreb (CISTEM 2022), Tunis, Tunisia. October 2022 (submited).

[2]. M. A. Barrios, H. Abubakr, V. Cárdenas, H. Miranda, J. Guerrero and J. C. Vasquez, "Converter for PV Systems with Medium-Frequency AC-Link and Storage Support," Interdisciplinary Conference on Mechanics, Computers and Electrics (ICMECE 2022), Barcelona, Spain. October 2022.

[3]. H. Abubakr, M. A. Barrios, S. Alghamdi, A. Milyani, A. Lashab, J. C. Vasquez and J. Guerrero, “Performance Assessment of Benban Solar Park and Zafarana Wind Farms on the Egyptian Transmission system” Interdisciplinary Conference on Mechanics, Computers and Electrics (ICMECE 2022), Barcelona, Spain. October 2022

[4]. M. A. Barrios, V. Cárdenas, J. M. Sandoval, J. M. Guerrero, and J. C. Vasquez, “A Cascaded DC-AC-AC Grid-Tied Converter for PV Plants with AC-Link,” Electronics, vol. 10, no. 4, p. 409, Feb. 2021.

[5]. J. M. Sandoval, V. Cárdenas, M. A. Barrios, M. G. Garcia, and J. Alcala, "Multiport Isolated link with Current-Fed Z-Source Converters to Manage Power Imbalance in PV Applications," Electronics, vol. 9, no. 2, p. 280, Feb. 2020.

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CHAPTER 2. PV SYSTEMS AND BATTERY ENERGY STORAGE SYSTEMS

Photovoltaic systems and energy storage systems are critical elements and factors for energy system decarbonization; therefore, understanding both technologies is essential. In this chapter, there is an introduction to both systems. First, by means of PV modeling, the inner working of a PV cell is presented alongside PV-array topologies and MPPT algorithms. Secondly, Battery systems deployment, battery technologies, and battery modeling are studied.

2.1. PV SYSTEMS

The photoelectric effect is the process of electrons liberation when a material is hit by electromagnetic radiation. Then, the photovoltaic effect is a particular example of the photoelectric effect, where the sunlight, composed of photons, hits a special material that excites an electron, and instead of this electron being ejected out of the material, it is actually absorbed by the material. The special material is Silicon, a semiconductor material. A photovoltaic cell is made of two silicon layers, one layer is negative or n-type, and the other is positive or p-type [21]. The movement of the excited electron between the layers creates a voltage potential.

2.1.1. PV MODEL

A photovoltaic cell behaves essentially like a power diode, but where the positive and negative (pn) junction is exposed with the aim that photons can hit it. An ideal PV module consists of a light-dependent current source in parallel with an ideal semiconductor diode model [22]. Figure 2.1 presents a model where the series (R_s) and shunt (R_p) resistances are included in the model.

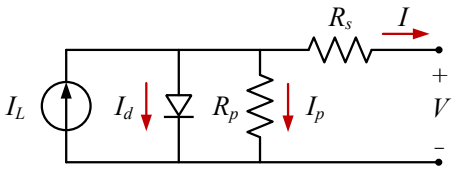


Figure 2.1: Rp PV model.

$$I = I_{ph} - I_d - I_p \tag{2.1}$$

The series resistance produces a voltage drop in the PV module, and the amplitude of the dropped voltage depends on the size of the resistor, which is usually small. The shunt resistor is added to the model to represent the current that flows from PV to the ground (leakage current) that circulates by the PV's frame. In contrast with R_s, R_p is usually high, and its effect can be noticed when the irradiance is low. The mathematical description for this model is given in (2.1), and the mathematical definition of I_{ph}, I_d, and I_p can be found in Appendix A.

Next, the power versus voltage (P-V) and the current versus voltage (I-V) characteristic curves of a commercial PV module are obtained by means of the equation (2.1). The specific PV module is produced by SolarWorld company, with part number SW 250 Poly [23]he PV's parameters are in Table 1.

Table 1: SW 250 Poly PV parameters.

Parameter	Variable	Value
Number of cells	N_s	60
Maximum Power	P_{max}	250 W
Voltage at P_{max}	$V_{(mpp)}$	30.5 V
Current at P_{max}	$I_{(mpp)}$	8.27 A
Open circuit voltage	V_{oc}	37.6 V
Short circuit current	I_{sc}	8.81 A
Saturation Current	I_{s0}	1.32e-8 A
Light Intensity	S	1000 W/m^2
Temperature reference	T_{ref}	25 °C
Band energy	E_g	1.12 eV
Shunt Resistance	R_p	1000 Ω
Series Resistance	R_s	0.01 Ω

Figure 2.2 and Figure 2.3 show the P-V and I-V characteristic curves, respectively, under five different solar irradiance levels, from 1000 W/m^2 to 200 W/m^2 with 200 W/m^2 steps. The major effect of the solar irradiance amount hit in the PV-module is the decrease of photocurrent, and this reduction depends on the irradiance level, which can be easily seen in Figure 2.2. Still, this effect is present in both figures. Another consequence of the irradiance level can be seen on the PV module's open-circuit, where this value is reduced if the irradiance is also decreased.

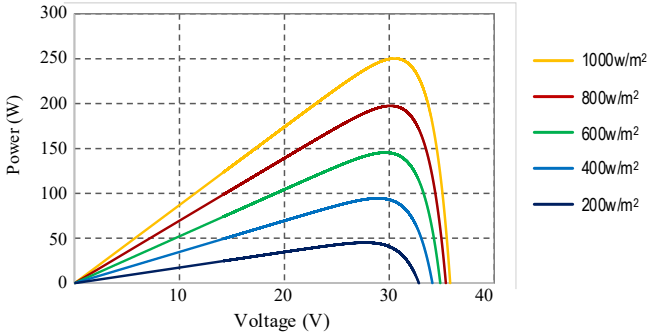


Figure 2.2: PV-module power versus voltage curves.

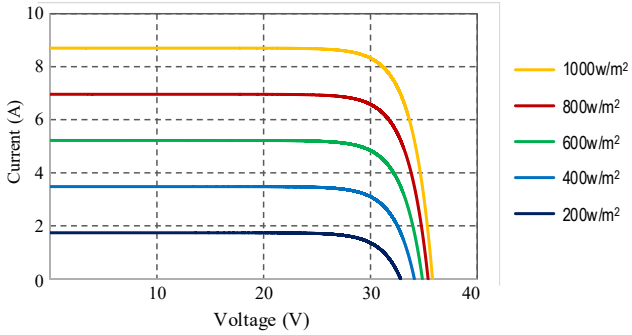


Figure 2.3: PV-module current versus voltage curve.

2.1.2. PV CONFIGURATION

PV systems have high modularity that allows them to be placed in different configurations or topologies by grouping or dividing them into arrays or strings that feed one or more power electronic converters. Each structure has distinct advantages and disadvantages, which the designer must consider to achieve a particular purpose.

The three most common configurations are centralized topology, string topology, and AC module topology [24]. There is another popular topology, but this one is made by combining the centralized and the string topology; this fourth topology is called multi-string topology and was developed for large-scale PV systems.

2.1.2.1 Centralized topology

The main characteristic of the centralized topology is that it uses only one inverter. This configuration is robust but not flexible. Some advantages of this topology are the straightforward structure and the use of a relatively simple control scheme for the power inverter. The regulator has the task of extracting the maximum power available

in the PV arrays at every moment and regulating injected current to the grid or the output voltage on a microgrid. This topology presents problematic aspects related to the poor exploitation of the available power in the PV modules under partial shading circumstances due to using a standalone MPPT. Other limitations are related to the mismatch losses between PV modules, high power losses on the string diodes, and low flexibility.

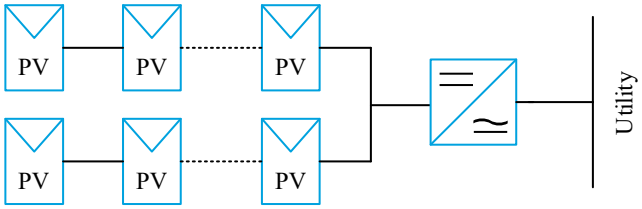


Figure 2.4: Centralized topology.

2.1.2.2 String topology

The string configuration uses one power converter per PV string; this is an outstanding improvement in harvesting PV energy. Among the advantages of this structure is the modular concept; this allows adding more PV modules without changing the size of the power inverter. No string diodes are required, and each string has its own MPPT; this is ideal under partial shading because the operating points of each string vary independently.

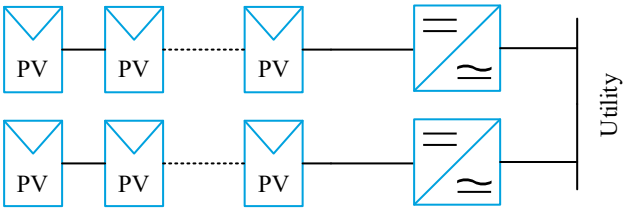


Figure 2.5: String topology.

2.1.2.3 AC modules topology

The AC module configuration, also called microinverter topology, is the structure that presents the most modularity (it is considered a plug-and-play configuration) as well as the best MPPT performance because each PV module integrates a dedicated power converter that runs its own MPP tracker. Another advantage of this structure is that the power mismatch between PV modules is reduced. The main disadvantage of this topology is that it requires a boost stage because the PV voltage is not enough to feed any AC grid. Another limitation of using this topology is that it is not suitable for large-scale installations; it is more oriented for houses or rooftop PV systems.

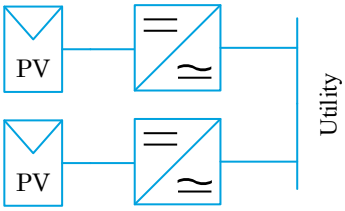


Figure 2.6: AC module topology.

2.1.2.4 Multi-string topology

To compensate for some disadvantages from the previous topologies, multi-string topologies were developed. This new structure takes some of the advantages of centralized and string topologies. Therefore, the MPP capabilities are improved because each string has a DC-DC converter running an MPP tracker; modularity improves as well. Hence, it is possible to attach a new string to the already installed strings without modifying the original setup. Each string will feed the already installed centralized inverter. When implementing this topology, the centralized inverter must be sized to allow modularity, considering the maximum power in the system.

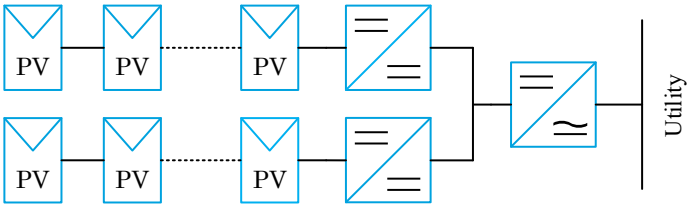


Figure 2.7: Multi-string topology.

2.1.3. MPPT

A PV module that works under uniform solar irradiance and temperature conditions presents characteristic P-V curves, as in Figure 2.2. At the peak of each curve, there is a single point *"x"* called the maximum power point, in which the PV module delivers the maximum available power for those set of environmental conditions; therefore, it works with the maximum performance.

When a load is directly attached to a PV module (directly coupled), the PV module's operation point is defined by the intersection of its characteristic P-V curve. In general, this operating point does not match the MPP.

In order to solve that problem, a DC-DC converter is inserted between the PV module and the load. The converter is provided with an MPPT algorithm that senses the PV module's voltage and current and automatically adjusts the duty cycle to maintain the

PV module's operating point at the MPP regardless of the load. Nevertheless, the location of the MPP in the P-V curve is not known a priori. This point must be located by employing mathematical operations on a model or using an MPP algorithm.

There are several MPPT routines reported in the literature [25] [26] [27] that focus on finding the MPP: perturb and observe (P&O), incremental conductance (INC), constant voltage (CV), fuzzy logic, neuronal networks, and others. The P&O and the INC are discussed next.

2.1.3.1 Perturb and Observe

The most widespread MPP algorithm is the P&O (Figure 2.8), this method is simple and easy to implement, but its limitations are well-known: trade-off between speed and accuracy, and inaccurate under fast-changing conditions. In this method, the PV module's output voltage is perturbed by a small increment. Next, the PV module's

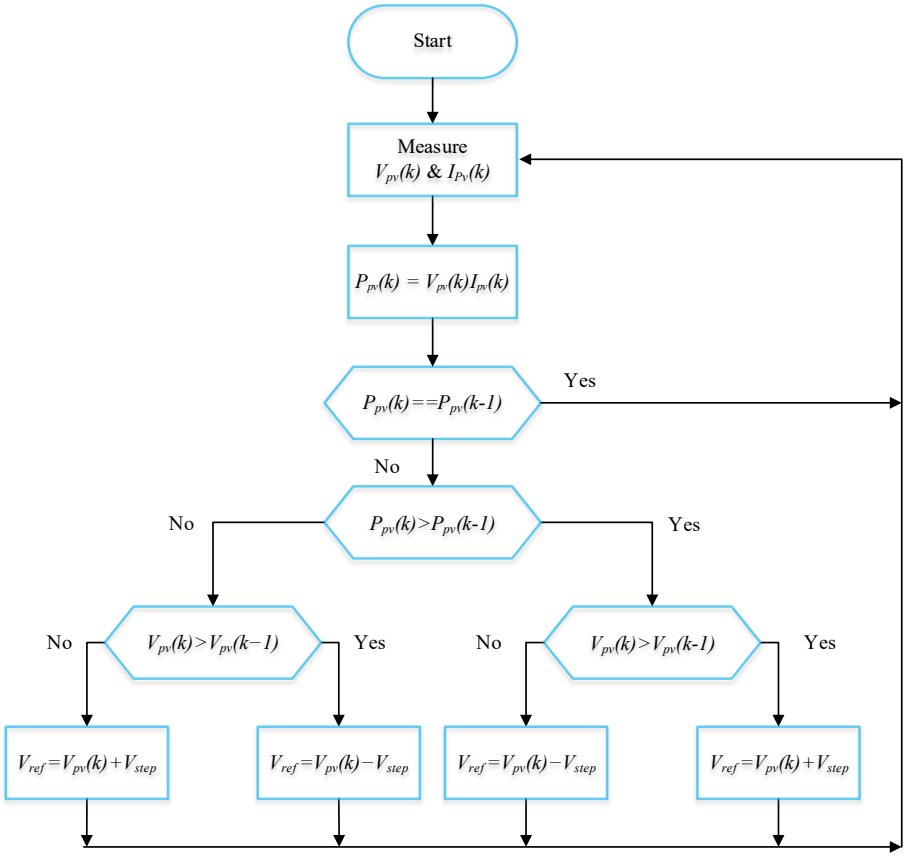


Figure 2.8: Perturb and observe MPP algorithm.

output power is measured to calculate the change in power ΔP (where Δ represent the difference between the kth sampled data and the $(k\text{-}1)$th sampled data), then the following condition is evaluated:

$$P + \Delta P > P \tag{2.2}$$

If that condition is true, it means that the operating point is near the MPP; therefore, the next perturbation must be done in the same direction in order to reach the MPP. If instead,

$$P + \Delta P < P \tag{2.3}$$

the new power value is less than the previous, then the operating point is far from the MPP, and therefore the next voltage perturbation must be done in the opposite direction. This approach ensures that the PV's harvested power will oscillate around the MPP. The oscillation is directly related to the step-size perturbation. The bigger the step size, the faster tracking of the MPP, in return, this leads to more considerable oscillations around the MPP, that is also translated to high power losses and poor performance of the MPP algorithm. There is another variable that affects the MPP performance, the perturbation frequency. The next perturbation must be done once the effects of the previous perturbation have disappeared; some works suggest that the perturbation frequency must be below the hundred hertz [28] [29] [30].

2.1.3.2 Incremental conductance

The incremental conductance method compares the instantaneous conductance (IC) to the incremental conductance of the PV module, equation (2.4) , and equation (2.5) , respectively. The equation (2.6) describes the operation principle of this method, the derivative of the output power with respect to the output voltage.

$$IC = \frac{I_{pv}}{V_{pv}} \tag{2.4}$$

$$INC = \frac{\Delta I_{pv}}{\Delta V_{pv}} \tag{2.5}$$

$$\frac{dP_{pv}}{dV_{pv}} = I_{pv} + V_{pv}\left(\frac{\Delta I_{pv}}{\Delta V_{pv}}\right) \tag{2.6}$$

The next three equations help determine where the algorithm is at the P-V curve and decide the direction of the next perturbation. At the MPP, the equation (2.7) is fulfilled. At the left side of the MPP or in the PV-module's low voltage zone, the

power's derivative will be positive, see equation (2.8) . On the contrary, being at the right side of the MPP (between the V_{mppt} and the V_{oc}) means that the derivative of power with respect to voltage is negative, see equation (2.9).

$$\text{if } \frac{dP_{pv}}{dV_{pv}} = 0, \text{ then } \frac{dI_{pv}}{dV_{pv}} = -\frac{I_{pv}}{V_{pv}} \tag{2.7}$$

$$\text{if } \frac{dP_{pv}}{dV_{pv}} > 0, \text{ then } \frac{dI_{pv}}{dV_{pv}} > -\frac{I_{pv}}{V_{pv}} \tag{2.8}$$

$$\text{if } \frac{dP_{pv}}{dV_{pv}} < 0, \text{ then } \frac{dI_{pv}}{dV_{pv}} < -\frac{I_{pv}}{V_{pv}} \tag{2.9}$$

The main advantage of the INC method is that it can track the MPP better than the P&O [8]. Another advantage is that the INC algorithm performs better than P&O under rapidly changing irradiance. Additionally, INC can detect when the MPP is found; therefore, the oscillation around this point has less impact on the losses and performance compared with the P&O algorithm. A restriction is that under a more significant step size, it will bring back the oscillations around the MPP during the perturbation. On the other hand, the INC algorithm has the disadvantage that instability can be triggered due to the use of the derivative operation in the algorithm; moreover, under minimal levels of irradiance, the differentiation process gets stiff, and it becomes sensitive to measurement noise.

2.2. BATTERY ENERGY STORAGE SYSTEMS

As renewable energies grow to a substantial level, the electric system will require more flexibility. In places with a high penetration of renewable energies, this energy will need to be stored for a few seconds, hours, or even more. Nowadays, the utility already requires many auxiliary services to guarantee trust and smooth operation. The auxiliary services allow the grid operator to react under unexpected changes in the demand, loss, or disconnection of large generators. In addition, the supply and demand must be balanced in real-time to ensure a quality power supply.

Globally, PV solar energy and wind energy have a limited impact on grid operation. However, once this kind of renewable energy reaches significant levels, the electric system will require more flexibility and fast response, which could be provided by employing energy storage systems.

The installed capacity of energy storage systems around the world in 2019 was 9 GW (see Figure 2.9). Pumped hydro plants represent 95% of the installed storage systems. Thermal storage systems are in second place with 3.3 GW. In third place, with 0.9% participation, the battery energy systems have 2.79 GW of installed capacity, but it is increasing yearly.

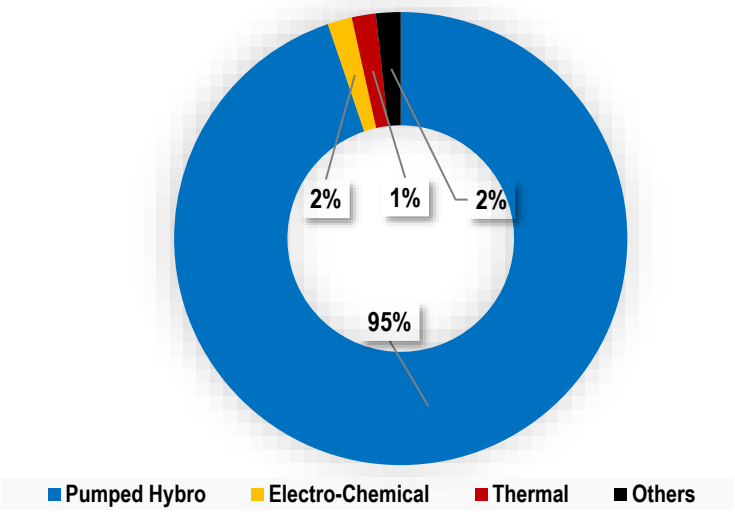


Figure 2.9: Global energy storage systems.

The battery energy storage system (BESS) in the stationary form can provide several numbers of storage services affordably. Still, today this way of storage is in the first steps regarding use or distribution stages. Considering that the cost of emerging technologies falls year by year, the storage systems become more competitive; therefore, auxiliary services like frequency regulation, voltage regulation, capacity reserve, and spinning reserve, among others, will increase in parallel as well as renewable penetration increase.

More than 1000 BESS projects (Figure 2.10) are registered in the Department of Energy (DOE) of the United States of America (USA). Considering all the services that can be provided with energy storage systems, 12% of those projects provide renewable capacity firming, equal to 1466 MW; 11% (962MW) of the projects offer electric energy time-shift, also known as shifting load. 10% deliver frequency regulation, and 8 % run voltage regulation; more data can be consulted on [31].

The wide range of auxiliary services offered to the grid by BESS allows those different battery technologies to prosper. Each battery technology has particular features that make them more suitable for providing certain auxiliary services than others.

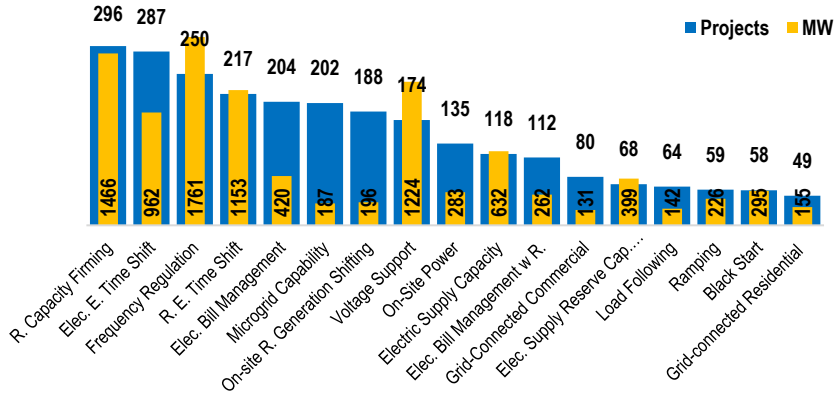


Figure 2.10: Battery energy storage projects: auxiliary services provided to the grid.

Some ancillary services require high power in a short period, for example, frequency response, while others require less power for long cycles like capacity firming. This variable access to the storage energy implies different charging and discharging rates; therefore, some technologies better fit certain kinds of ancillary services than others because of their performance or price.

In Figure 2.11, it is appreciated that each stacked bar represents one of the eight most frequent services that the battery storage systems offer to the utility; at the same time, each stacked bar is split into four sections, each section represents one of the four battery technologies most used globally. For example, the voltage support service has 174 projects, and those are divided in the following way, 16 projects opted to use flow batteries, 18 projects implemented lead-acid batteries, other 16 projects selected high-temperature batteries, also known as NaS batteries, and 97 projects instead implemented lithium batteries. The rest of the projects decided to use different battery technologies that are less relevant than those mentioned here.

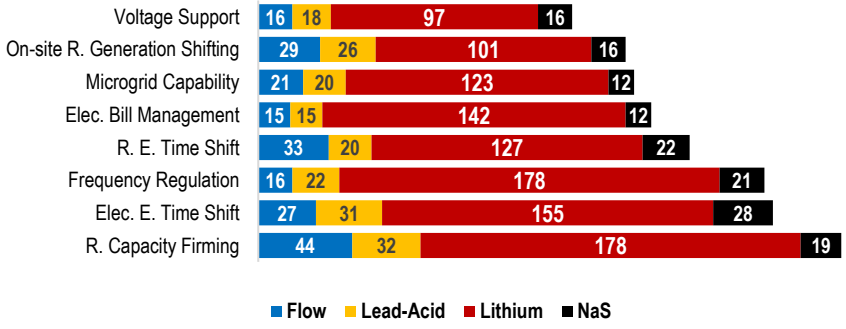


Figure 2.11: Number of projects sorted by auxiliary service provided to the grid and sub sorted by technology type.

To understand better how the ancillary services are distributed and the power levels where they are implemented, refer to Figure 2.12. In this figure, each stacked bar represents one of the eight most common auxiliary services given to the grid; then, each bar is split between six power levels. This figure represents valuable information, with which a first approximation can be obtained about what services could be provided to the grid according to the power levels. The figure shows that voltage support has been implemented at high-power levels, starting from 1 MW, where 81 % of the projects concentrate between 1 to 10 MW. A similar pattern is followed by frequency regulation, where BESS projects supporting this service are at power levels beginning from 1 MW. On the other hand, services like grid-connected residential can only be provided at low power levels, for example, below 10 kW. Additional services like microgrid capability are only available for power below 1 MW.

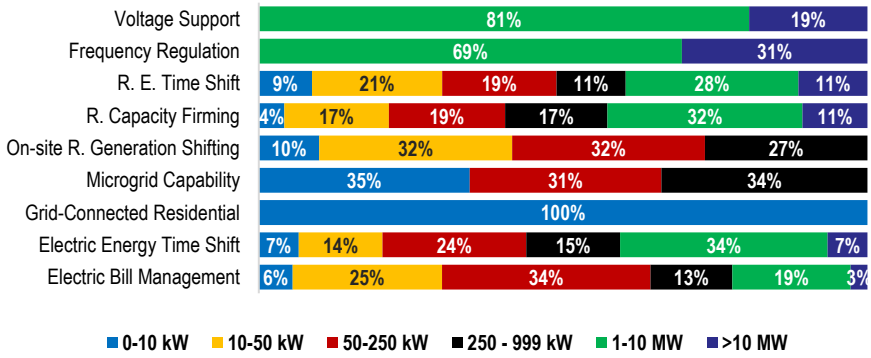


Figure 2.12: Total projects classified by power range and battery technology.

2.2.1. BATTERY TECHNOLOGIES

Nowadays, electrochemical storage is one of the most growing markets in the storage segment. Especially lithium-based batteries have had impressive investments and developments, which is why most of the projects presented in the last section implemented them. Perhaps, there are other chemical technologies with promising features, like high-temp batteries or flow batteries.

As previously mentioned, electrochemical storage technologies have different intrinsic properties that make them suitable in technical terms for specific applications. As a result, they can deliver specific services to the grid optimally. Depending on the characteristics of the batteries, like charging time, discharging rates, capacity, output power, and others, some applications are ideal for providing specific ancillary services to the utility than others. In addition to the previous characteristics, there are others where the relationship between the specific energy and specific power that can hinder the use of particular battery technologies in some applications or, on the other hand, can favor others.

Lithium-ion batteries have high specific energy and power; this explains why they are extensively used in an undefined number of applications, from wearable devices to grid support. Nevertheless, there are applications where the BESS is not required to fulfill high power and high-capacity features, but others are more interesting; for example, stationary applications would consider more important charging and discharging rates. A brief classification of the electrochemical storage system is shown below; this classification is divided into four categories: lithium batteries, acid-led batteries, high-temperature batteries, and flow batteries.

- Lithium batteries
  - NMC/LMO: nickel manganese cobalt oxide/lithium manganese oxide
  - NCA: nickel cobalt aluminum oxide
  - LFP: lithium iron phosphate (lithium ferro-phosphate)
  - LTO: lithium titanate
- Lead-acid batteries:
  - Flooded
  - VRLA: valve-regulated lead-acid
- High-temp batteries:
  - NaNiCl: sodium nickel chloride
  - NaS: sodium-sulfur
- Flow batteries:
  - ZBFB: zinc-bromine
  - VRFB: vanadium redox flow battery
  - Zn/Fe: zinc-iron

Table 2: Battery technology comparison table.

BATTERY TYPE	Life time (years)	Cycles (x1000)	DOD (%)	In. Costs $/kWh	Op. Costs ($/kWh)	Power Density (W/L)	Energy Density (Wh/L))	Efficiency (%)	Auto Discharge (%)	Safety	Construction (years)	C Rate
VRFB	12	10	100	268	11	2	42.5	72	0.15	H	1	1/4
ZBFB	10	4	100	696	15	13	45	72	15.0	M	1	1/4
NaNiCl2	15	3.5	100	323	8	210	215	85	5.00	M	0.5	1/6
NaS	17	5	100	436	8	140	220	81	0.05	M	0.5	1/6
Flooded	9	1.5	50	147	3	355	75	82	0.25	H	0.3	2
VRLA	9	0.5	50	226	3	355	75	80	0.25	H	0.3	2
LFP	12	3.5	90	466	8	5050	410	86	0.10	H	0.5	2
LTO	15	10	95	880	6	5050	410	96	0.05	H	0.5	10
NCA	12	1.5	90	284	8	5050	410	92	0.20	L	0.5	1
NMC	12	3.5	90	339	8	5050	470	92	0.10	M	0.5	2

Table 2 shows the most significant specifications from the four battery technologies presented in this chapter. A brief description of the four battery technologies is introduced next.

2.2.1.1 Flow batteries

One of the most mature technologies regarding flow batteries is vanadium redox flow. This technology reconsiders the zinc-chloride batteries, but now with a new approach and a better selection of chemical solutions than before. This battery technology can also be described as regenerative fuel cells, and a variety of them exist. This battery technology differs from others because the electroactive material is not stored inside the electrode. The electrolyte is stored in different tanks, one is for the anode, and one is for the cathode. Some advantages of the flow batteries are: operation near the ambient temperature, they can be scaled up in power density and reach a high life cycle (10000), the raw materials are cheap, and they have high deep discharge cycles without impact in the life cycle and are considered secure. Some disadvantages include low efficiency compared with lithium-ion batteries, complex installation, high installation cost, and maintenance; therefore, these batteries are only used in stationary applications.

2.2.1.2 High-temperature batteries

These batteries are called high-temperature batteries because they require high temperatures to keep the active material in a liquid state. Typically, the anode material is a molten sodium structure; therefore, this family type of battery is called sodium beta battery. In the case of sodium sulfate, the cathode is composed of molten sulfur in the most common configuration. The NaS batteries typically operate between 300 and 350 °C, whereas Sodium–nickel chloride batteries operate between 250 and 350 °C. Some of the advantages of this technology include a relatively high energy density compared to Redox flow or Lead-acid batteries (140 Wh/l and 300 Wh/l), and high power density (140 W/l). This type of battery is suitable for daily duty cycles, and it can be discharged for long periods or provide substantial power peaks. Auto-discharge is limited (0.05% and 1%), long cycle life (5000-10000). The main disadvantage of this technology is the annual operating cost; moreover, heating the solution drains nearly 3% of the installed power in a steady-state.

2.2.1.3 Lead-acid batteries

This battery technology was developed more than 150 years ago; it is the most mature and the most widespread worldwide. These batteries have a reasonable price-performance in a wide range of applications. However, they have a low energy density, are heavy, and usually do not respond well to deep discharge. Moreover, lead is considered a restricted material in many countries; however, they have a significant market. There are only two lead-acid battery types: the flooded and sealed versions.

From these two options, flooded batteries are cheaper and more mature than its counterpart, but they have not been implemented widely in delivering auxiliary services to the grid. These technologies' most well-known related problems include low cycle life and poor efficiency. Another drawback of these batteries is that they release chemicals while being charged. Additionally, they lost water, which needs to be replaced. Self-discharge is limited to 0.09% and 4.0%, density energy between 50 and 100 Wh/l, and life span between 3 and 15 years; however, these batteries have a calendar life between 3 and 15 years, whereas the cycle life is from 250 to 2500 cycles.

2.2.1.4 Lithium-ion batteries

Sony Energy introduced these batteries in 1990. There are two groups of lithium batteries, Lithium-metal and Lithium-ion, and this classification depends on the anode's material. In the first group with Lithium-metal anode, there are two other subfamilies; these subfamilies rely on the material of the electrolyte, based on Liquid Electrolyte are Li-metal Liquid batteries, and based Polymer electrolytes are Li-metal Polymer batteries. In the other group with Lithium-ion anode, there are two subfamilies, based on Liquid electrolytes are found the Li-ion Liquid batteries, and based on Polymer electrolytes are the Li-ion Polymer batteries. Notwithstanding those batteries based on polymer electrolyte batteries that were designed in the 1970s, the most common electrolyte is based on Li-ion liquid, a combination of liquid organic solvent mixed with lithium salts.

Among their advantages, it can be found that they present high specific energy (W/kg), high energy density (Wh/l), and high energy power (W/l). Additionally, they can handle a superior number of life cycles, high efficiency, high rate, a relatively long lifetime, and low auto-discharge characteristic. Lithium batteries show problems when they are implemented outdoors, where ambient temperatures are high. Moreover, there are thermal issues from the stability and safety point of view; in some cases, the batteries can catch fire due to leaks or smoke fast venting from the cell. In addition, they do not adequately handle overcharge or over-discharge conditions; therefore, Battery Management System (BMS) is required to monitor the battery's voltages and temperatures.

Within the family of lithium batteries, a wide variety of sub-chemicals are mixed with lithium to develop specific characteristics such as high power density, high energy density, or long life cycles. Still, this discussion goes beyond the scope of this work. Table 3 [32] indicates the appropriateness of the US stationary energy storage technologies described in the previous section considering reduced typical applications. The table ranks the battery technologies, where 100 is the most suitable and 0 is the less appropriate technology for the given service.

Recent research [33] on US battery grid storage solutions have projected 2021 costs for fully installed 100 MW, 10-hour battery systems of: lithium-ion LFP ($356/kWh)

and lithium-ion NMC ($366/kWh); therefore, the LFP batteries are 2.8% cheaper than NMC batteries. Even though LFP batteries are cheaper than NCM batteries, NCM technology still are considered as a better solution to provide grid services to the grid (Table 3).

Table 3: Battery technology application raking.

BATTERY TYPE	Renewable shifting	Renewable Smooting	Flex Ramping	Anciallilary Services	T&D Deferral	Reactive Power Managment	BTM Power Managment
VRFB	33	17	33	17	33	18	33
ZBFB	8	0	8	0	8	0	25
$NaNiCl_2$	42	8	42	8	42	17	42
NaS	50	25	50	25	58	25	50
Flooded	20	50	20	50	75	70	70
VRLA	17	50	17	50	75	67	67
LFP	58	83	58	83	67	75	75
LTO	25	67	25	67	50	58	58
NCA	75	75	75	75	83	83	83
NMC	83	92	83	92	92	92	92

2.2.2. BATTERY MODEL

BESS is a prominent solution that is getting more affordable and able to address several technical challenges of renewable energy integration, for example, the variability and uncertainty of solar energy. In this work, batteries were selected due to their unique capabilities to absorb, store and then reinject the energy efficiently. As explained in previous sections, some battery technologies are intrinsically more suitable for a particular task. For instance, lithium-ion batteries have proven to have a fast response, high efficiency, a good depth of discharge, and a high power density.

It is necessary to have a mathematical model that estimates a battery's quantitative behavior and then reproduces and controls it. There are two kinds of battery mathematical models: electrochemical and electric models. The electrochemical modeling of a battery is structurally based on the internal chemical reactions of the cell. This kind of modeling is precise, but its main disadvantage is that it is complex, and it is necessary for accurate identification of the internal electrochemical process of the cell. In addition, it requires a specific characterization that will require specialized laboratory equipment that is expensive by nature, like frequency response

analyzers, calorimeters, temperature exchangers, and electrochemical equipment for post-mortem analysis.

The model based on electric circuits is widely used in many works, and it is another way to represent the battery behavior using passive linear components (resistances, inductances, capacitances). For instance, some models represent the battery capacity employing a capacitor. Due to the voltage and internal resistance dependent on the temperature and the state of charge (SOC), some models represent the battery's open-circuit voltage (V_{oc}) as a controlled voltage source plus a variable resistance, both dependent on the SOC and temperature. There is a wide variety of mathematical models based on an electrical circuit and other approximations. Therefore, the electric model is selected in this work because it is simple to obtain and implement.

2.2.2.1 Model-based on Shepherd equation

This mathematical model (Figure 2.13) describes the battery behavior directly in terms of the terminal voltage, open-circuit voltage, internal resistance, discharge current, and SOC; additionally, this model represents the charge and discharge process of the battery [34]. This model only requires the SOC as a state variable to reproduce the datasheet charging and discharging curves. The battery model is implemented using a controlled voltage source in series with a resistance representing the battery's V_{oc} *and* internal resistance R, respectively. The equation (2.10) describes the generic mathematical model based on the work developed by Shepherd.

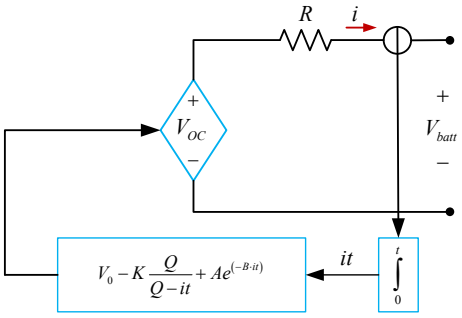


Figure 2.13: Sthepherd battery model.

$$V_{oc} = V_0 - K\frac{Q}{Q - it} + Ae^{-B\cdot it} \tag{2.10}$$

Where:

- V_0 is the battery voltage constant [V].
- K is the polarization constant [V/(Ah)].
- Q is battery capacity in [Ah].

- *it* is the actual battery charge [Ah].
- *A* is exponential zone amplitude [V].
- *B* is the exponential zone time constant inverse $[Ah]^{-1}$.
- *i* is the battery current given in [A].

The SOC is the ratio *it/Q*. To calculate *it* is necessary to integrate the battery current and consider the initial capacity of the battery:

$$Q_0 + \int_0^t -i\,dt = it \tag{2.11}$$

More details about this battery model are found in Appendix B.

A new mathematical model (Figure 2.14) based on the Shepherd equation was developed in [35] by Oliver Tremblay et al. Its main advantage is that it can better describe the battery behavior than the model proposed in the equation (2.10). This new model can represent the battery voltage dynamic with better precision when its current is not constant and consider the open-circuit voltage (V_{oc}) as a function of SOC. A new term (polarization voltage) is added to the equation (2.10) to represent the VOC better. Additionally, the polarization term that was modified for the equation (2.10) is again adjusted to accomplish a better performance. The new equation for this battery model is described by

$$V_{OC} = V_0 - K\frac{Q}{Q-it}\cdot it + Ae^{-B\cdot it} - K\frac{Q}{Q-it}\cdot i^* \tag{2.12}$$

The last equation's variable definitions are the same as from its counterpart equation (2.10). In addition, there is a new variable i^* called filtered current; this is the current that flows through the polarization resistance. The filtered current solves the algebraic

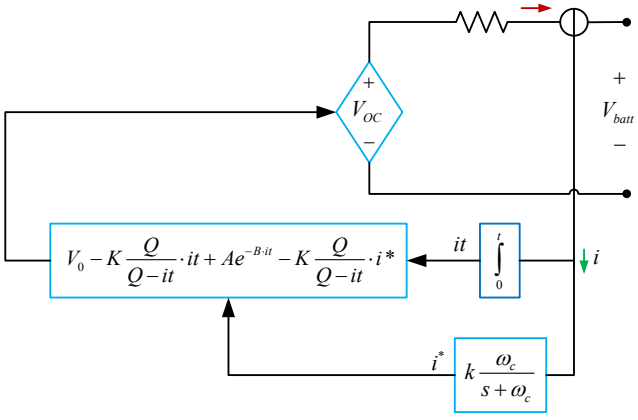


Figure 2.14: Tremblay's battery model.

loop presented in the Shepherd equation. Due to the polarization voltage term of the equation (2.12), the V_{OC} changes nonlinearly with the SOC.

There is a difference between the model for discharging and charging mode, and this is due to the behavior of the end of the charge point, where the voltage ramps up quickly when the battery is up to be fully charged ($it \approx 0$). This behavior is represented by the polarization resistance (equation (2.13)), which increases immediately as well.

$$PR = K\frac{Q}{it - 0.1Q} \tag{2.13}$$

Therefore, the equation for a Li-ion battery in charge mode is represented by

$$V_{OC} = V_0 - K\frac{Q}{Q - it}\cdot it + Ae^{-B\cdot it} - K\frac{Q}{it - 0.1Q}\cdot i^* \tag{2.14}$$

Some considerations on this improved battery model are as well as the previous model found in Appendix B.

2.2.2.2 Battery model comparison

Figure 2.15 shows a simulation comparing the battery model described by equation (2.10) and (2.12). As is expected, the battery model represented by the equation (2.10) cannot describe some electrical behaviors that occur in actual operation. In both cases, the battery under test is the Panasonic NCR18650GA.

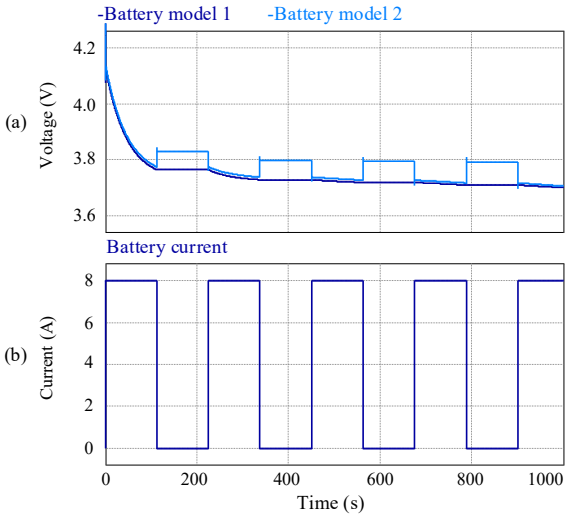


Figure 2.15: Battery model comparison.

The test consists of extracting a periodically pulsed current with an amplitude of 8 A each 255.22 seconds. The main misbehavior is that when the current extracted from the battery stops, the voltage does not suffer any alteration; in contrast, the battery model characterized by the equation (2.12) can represent the aforementioned effect just after the current stops flowing through the battery, at that moment the battery voltage is recovered. In an actual battery, similar behavior must happen when the battery current resumes; at that moment, the battery voltage must drop as the second battery model does, an effect that the first battery model cannot reproduce. Therefore, it can be said that the second battery model represents the battery behavior more effectively than the equation (2.10); thus, this is the model that this work will use for the subsequent simulations with energy storage units, and its parameter are found in Table 10.

2.2.3. ENERGY STORAGE COUPLING

Basically, there are two coupling schemes for adding battery energy storage systems to a new or existing electrical system based on renewable energies: AC coupling or DC coupling. Next, some characteristics of both methods are described.

2.2.3.1 AC-Coupling

A traditional PV-system generator interconnected to the utility that wants to add energy storage to its system will require two power inverters, one attached to the PV system and the other connected to the energy storage system. Figure 2.16 shows how both systems are commonly interconnected between them and towards the utility under an isolation scheme. This configuration could occur on-site, next to each other, or the BESS can be installed in a different place far away from the PV farm.

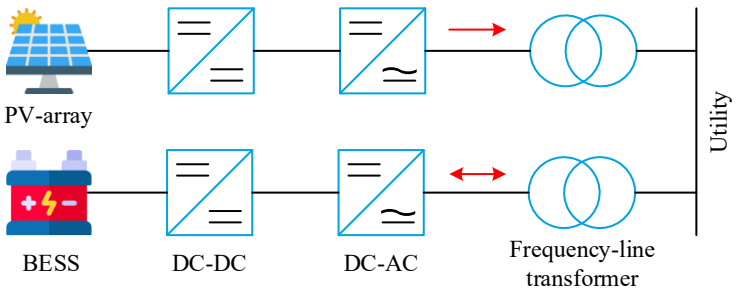


Figure 2.16: AC-coupling for energy storage systems.

With this configuration, the injected power to the grid can be maximized by means of both energy sources, the PV and the BESS. This schema is simple but requires more installation costs due to using another set of power converters and an additional transformer (when grid operators need isolation); therefore, the system could have

more power losses [36]. PV systems coupled in AC are pretty simple and reliable [37], and are the most used scheme globally despite their intrinsic disadvantages [38].

2.2.3.2 DC-Coupling

This kind of coupling (Figure 2.16) has not been widely implemented in comparison with AC coupling. New projects can use DC coupling, as well as deployed PV projects can use DC coupling to add energy storage to their system. DC coupling has some advantages: easy use of DC power sources and storage devices [38], increasing energy revenue, lower balance of system (BOS) or balance of plant cost [39], and better efficiency [40]. Compared with AC coupling, DC coupling only requires one bidirectional power inverter, allowing power to flow between the DC side and the AC side.

Next, Table 4 compares each option's coupling, PV harvesting, and revenue possibilities. Additionally, Table 5 shows the advantages and disadvantages of such coupling methods.

Table 4: Harvesting and revenue possibilities.

PV HARVESTING / COUPLING	DC	AC
CAPACITY FIRMING	+	+
ENERGY TIME SHIFTING	+	+
CLIPPING RECAPTURE	+	-
CURTAILMENT RECAPTURE	+	-
LOW VOLTAGE HARVEST	+	-
RAMP RATE CONTROL	+	+

Table 5: Advantages and disadvantages on coupling methods.

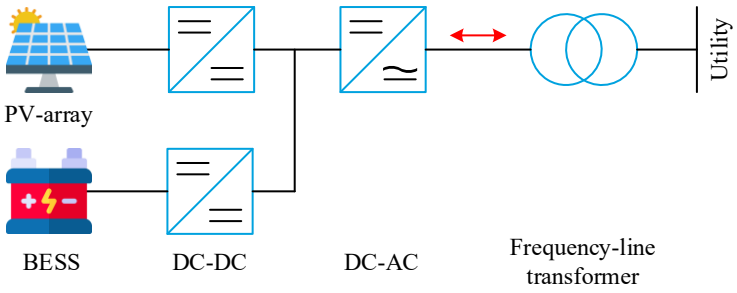


Figure 2.17: DC-coupling for energy storage systems.

CHARACTERISTIC / COUPLING	DC	AC
LOW INSTALLATION COST	+	-
CO-LOCATION	+	+
STAND-ALONE	-	+
ADAPT TO EXISTING PV SYSTEM	-	+
RELIABILITY	-	+
EFFICIENCY	+	-
REVENUE	+	-
BENEFIT/COST	+	-

2.2.4. PV PLUS STORAGE POSSIBILITIES

Most of the large-scale PV systems around the world do not have an energy storage system that allows them to expand production hours or maximize the utilization of the energy generated by the PV farm. Adding storage coupled in DC or AC enables different ways to exploit the energy in the PV modules. Next, some ways to take full advantage of the PV system plus BESS are examined.

2.2.4.1 Capacity firming

Due to the intermittency of photovoltaic solar energy, having energy storage allows the PV system to guarantee constant power production. PV + BESS makes PV generation dispatchable as a combined-cycle gas turbine or a coal plant, giving the system the characteristic of adjusting the power injection to the grid as far as possible.

2.2.4.2 Energy time shifting

Storing energy allows controlling the harvested energy from PV modules and injecting it when it is more advisable. For example, when PPA rates are higher or when demand falls outside periods of PV generation, then with BESS, it is possible to store energy and inject it at will. Refers to Figure 1.5 to see how the energy time-shifting is done.

2.2.4.3 Peak shaving

Commonly, installed PV arrays energy's capacity is higher than the power electronic inverter's capacity, this rate represented by the equation (2.15) goes from 1.25 to 1.5.

$$\text{Array to inverter ratio} = \frac{\text{Array power rating}}{\text{Inverter rating}} \tag{2.15}$$

Then, when the solar irradiance is full, the PV inverter will clip (Figure 2.18) the exceeded power by, for example lowering the DC input current, which produces the DC voltage rising above the maximum power point voltage, thereby reducing the PV modules output power; otherwise, the power inverter will be overloaded. With energy storage, the clipped energy is stored instead of being lost; later, the saved energy can be injected into the grid at an appropriate time. For its nature, peak shaving capability is only available under DC-coupled systems.

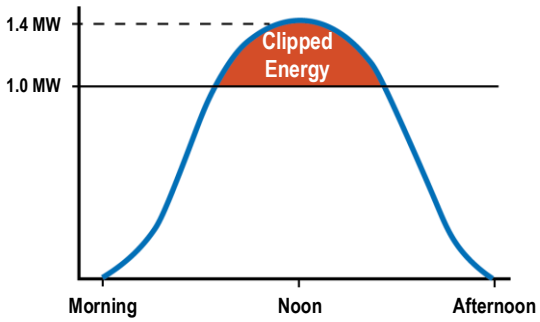


Figure 2.18: Peak shaving recapture.

2.2.4.4 Ramp rate

The grid usually requires the power ramp rate restriction (Figure 2.19) to mitigate any sudden impact of power injected towards the utility due to a generator connection. This also happens when suddenly a generator is disconnected from the grid for any reason like intermittence, voltage, or frequency drift. This restriction makes the PV farms inject a specific ramp rate power imposed by the grid by clipping the available power on the PV arrays. As in the peak shaving case, the clipped energy can be stored for later use that, otherwise could have been lost.

2.2.4.5 Low power harvesting

PV power inverters usually require a minimum input voltage to start to operate. This implies that the available power from the PV farms in the morning or near the night, when the irradiance is low, cannot be injected into the grid because the voltage in the inverter's input is not enough to start the operation of the inverter. The previous behavior can also be faced with a high partial shading in the PV farm (Figure 2.20). The inverter is off-grid in the situations mentioned above, and the PV farm's available energy is not injected into the grid. With DC-coupled energy storage systems, the energy potentially lost can be captured.

As renewable energies participation continues increasing, the grid operators and the stakeholder will consider the energy storage system as a critical tool for renewable energy integration, facilitating the energy transition by providing ancillary services to the grid supported by energy storage systems. In the same sense, renewable farm operators are taking advantage of the storage systems to maximize the capture of renewable energies under conditions where the energy will be lost without a storage solution.

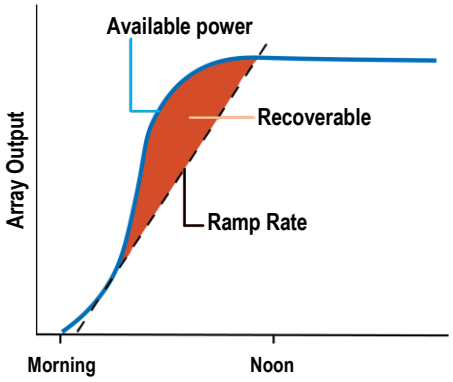


Figure 2.19: Ramp rate harvesting.

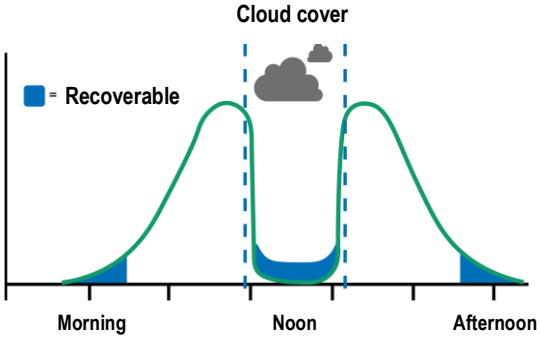


Figure 2.20: Low voltage harvesting.

CHAPTER 3. DC-DC CONVERTER FOR PV APPLICATION WITH ESS BASED ON 3L CONVERTER

The BESS coupled in DC uses a bidirectional DC-DC (BDC) converter parallel to the DC bus. This connection is made behind the main DC-AC converter. In addition to the advantages mentioned in the previous chapter, the DC coupling systems do not require a synchronization stage to interconnect the ESS to the PV system. Moreover, there is a direct coupling between renewable energies with DC output and BESS systems. Therefore, DC coupling is preferred when the output of multiple energy sources and loads is DC.

3.1. STATE OF THE ART

In the literature, there are plenty of bidirectional DC-DC converters; some of them are listed next:

- Bidirectional buck-boost converter [41]
- Cascaded buck-boost converter [42]
- Cuk converter [43]
- Quadratic buck-boost converter [44]
- Half-bridge converter [45]
- 3L bidirectional converter [46]

3.1.1. BIDIRECTIONAL BUCK BOOST CONVERTER (BBBC)

This converter (Figure 3.1) is derived from the conventional buck-boost converter; the difference consists of replacing the diodes with active switches, which will allow the bidirectional power flow. The switch Q_2 is off in the boost stage, while Q_1 is on. On the contrary, the switch Q_1 is off, while Q_2 is on when the converter works as a buck converter. When this converter is operated in continuous conduction mode

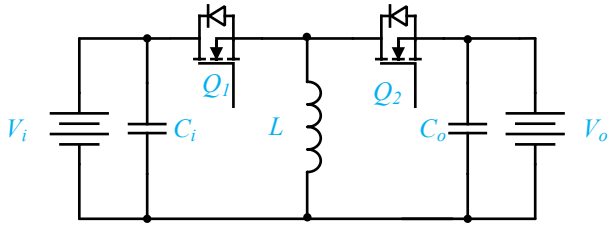


Figure 3.1: Bidirectional Buck and Boost converter.

(CCM), it presents a low efficiency when it is hard switched by common pulse width modulation (PWM). Unlike the buck or boost converters, the output voltage of the BBBC is negative while there is a positive input voltage. A disadvantage of this bidirectional converter is that the switches have to block the input voltage plus the output voltage.

3.1.2. CASCADED BUCK BOOST CONVERTER (CBBC)

The converter of the Figure 3.2 can be obtained by cascading the buck and boost bidirectional converters. The CBBC works on the four quadrants; in other words, it can boost and buck the voltage in both directions. One disadvantage is related to the number of active semiconductors that complicate its control. The combination of the switches plus the current direction allows the input voltage to step up or down. In the boost mode, Q_2 and Q_4 are always turned off, Q_1 is always turned on, while PWM is switching the switch Q_3. In buck mode Q_2, Q_3, and Q_4 stay turned off, while Q_1 is operated by the PWM [47]. Each switch has to block the input voltage.

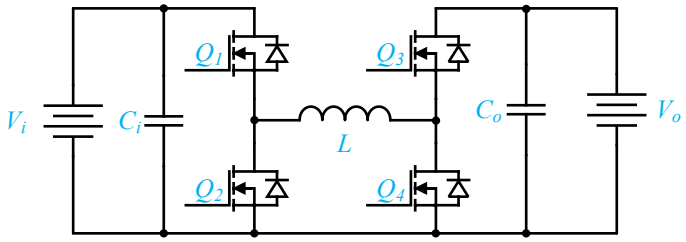


Figure 3.2: Cascaded buck-boost topology.

3.1.3. BIDIRECTIONAL CUK CONVERTER (BCC)

The bidirectional Cuk converter (Figure 3.3) is based on the classic Cuk converter. It is built by replacing the unidirectional switches with bidirectional switches. In this converter, two switches are always active. Capacitors C_i and C_o work as coupling capacitors, while capacitor C is an energy storage device. The Cuk converter can operate with voltages greater or lower than the input voltage. The main advantage of this converter is that the current ripple, either the input or the output is small; thereby, it is suitable for battery banks or capacitors [48]. During the step-up mode, the Q_1 is active, and Q_2 is inactive; on the other hand, when stepping down the voltage, the switch Q_2 is active, and Q_1 is inactive. As CBBC, the switches of the BCC have to block the input plus the output voltage, making the blocking voltage (BV) rate for both topologies a clear disadvantage against the other converters.

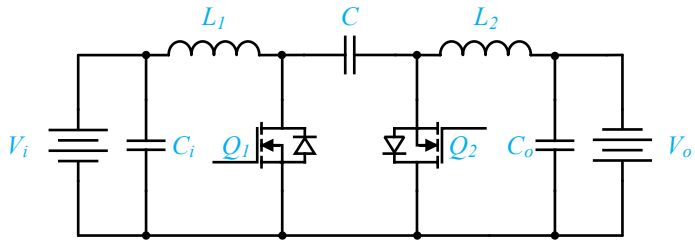


Figure 3.3: Bidirectional Cuk converter.

3.1.4. QUADRATIC BUCK BOOST CONVERTER (QBBC)

The main feature of the QBBC converter (Figure 3.4) is that it can generate high conversion gains either in boost mode or in buck mode. Other converters can get high voltage gains but have high duty cycles and high switching frequency, which translates into high power losses. Another feature is that this converter presents a reduced current ripple. Moreover, this converter offers a simple control strategy because only one switch is commuted during each stage (buck or boost). The converter is built with four active switches, two passive switches, two inductors, and one flying capacitor. One disadvantage of this converter is that it presents a low efficiency if it is hard switched; additionally, each device has to block the input voltage.

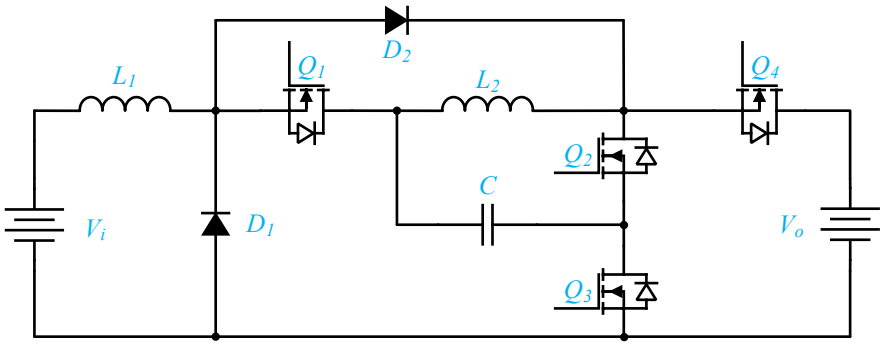


Figure 3.4: Quadratic buck-boost converter.

3.1.5. HALF-BRIDGE CONVERTER (HBC)

The HBC depicted on Figure 3.5 is the most common bidirectional converter. Practically, it combines a boost converter and a buck converter attached in antiparallel way [49]. It can work in boost or buck mode with power transfers on both sides. The converter's behavior is explained briefly next. Switch Q_1 works following the duty cycle during the step-down voltage conversion, whereas switch Q_2 is inactive, but its associated antiparallel diode is working. Similarly, during the step-up voltage

conversion, duty cycle controls switch Q_2, and Q_1 is inactive. An advantage of this converter compared to the buck-boost converter is that the half-bridge converter only requires the half of active components, and compared to the Cuk converter, the half-bridge converter only needs one inductor to operate. In contrast with the bidirectional Cuk converter, the HBC's switches only block the input voltage.

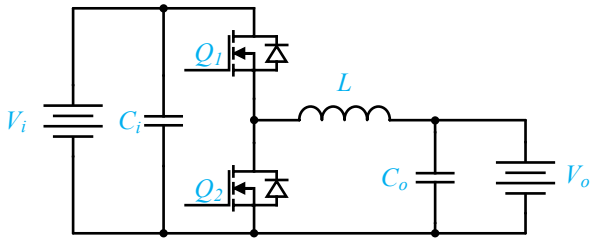


Figure 3.5: Half-bridge converter.

3.1.6. BIDIRECTIONAL 3L CONVERTER

The three-level (3L) DC-DC converters are derived from the conventional 2L DC-DC converters [50]. The objective of 3L converters is to reduce the voltage stress presented in 2L converter switches. On 3L DC-AC converters, the phase leg generates three levels of voltages, but this is not the case with DC-DC converters, where the name of 3L was adopted because of the similitude of how the devices are placed in the converter, as well as the feature of the converter's switches to block only half of the DC voltage.

The 3L BDC converter depicted in Figure 3.6 is derived from the half-bridge converter. It can operate in step-down voltage conversion where current flows from the high voltage (HV) side to the low voltage (LV) side and in step-up voltage conversion from LV to HV.

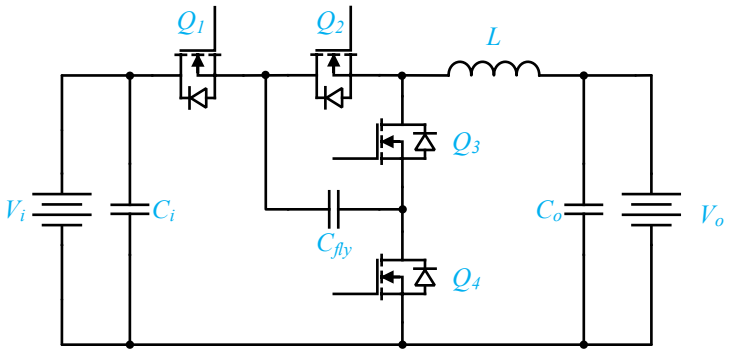


Figure 3.6: 3L bidirectional converter.

Four active switches integrate this converter; it requires one inductor and one flying capacitor, and two decoupling capacitors as any other DC converter. The 3L configuration of this converter presents some advantages; for example, the reduced voltage stress on the switches, the inductor's size can be minimized, and small current ripple on the inductor.

3.1.7. COMPARISON OF THE BIDIRECTIONAL CONVERTERS

A comparison of the reviewed bidirectional converters is summarized in Table 7 and Table 8. The common parameters between converters are listed in Table 6, while other and the particular parameters for each converter are registered in Table 7. The comparison is made considering that the converters work in buck mode, supplying energy from a regulated DC BUS to a resistive load. The converter's inductance and capacitance were selected such that the maximum inductor's current ripple is approximately 4 A, and the capacitor's voltage ripple is below 3% respectively.

Table 6: Converter's parameters.

Parameter	Variable	Value
Input voltage	V_i	120 V
Output voltage	V_L	39 V
Output current	I_{ch}	22.84 A
Switching frequency	f_{sw}	100 kHz
Capacitance	C	100 µF
Inductance	L	59.7 µH

Figure 3.7 presents the open loop simulation results. On the top part of the figure are the output voltages for the six converters, all of them reached the consigned output voltage of 39 V. The main difference is the initial overshoot, where the BCC has the most significant overshoot, around 110 %, with a rise time of 500 µs, and the QBBC has the best performance with 34% of overshoot and a rise time of 300 µs. More details are listed in Table 7. The bottom part of the previous figure is related to the inductor's current. As in the voltage waveform, the BCC has the most prominent current overshoot with a peak of 60.95 A at 302 µs. Once again, the QBBC has the smallest overshoot (107 %) with a rise time of 135 µs.

Table 7: Comparison table for the bidirectional converters.

FEATURE	BBBC	CBBC	BCC	QBBC	HBC	3L BDC
DUTY CYCLE	0.245	0.325	0.245	0.57	0.325	0.325
OVERSHOOT (V)	38 %	48 %	110 %	34%	47 %	48 %
RISE TIME (V)	330 µs	246 µs	500 µs	307 µs	246 µs	248 µs
OVERSHOOT (I)	170 % 57.9A	155 % 58.2A	170 % 61.6A	107 % 47.3A	155 % 58.2A	148 % 56.6
RISE TIME (I)	201 µs	143 µs	292 µs	135 µs	143 µs	141 µs
CURRENT RIPPLE	4.93 A	4.41 A	4.93 A	2.80 A	4.41 A	1.14 A
L [µH] (Δ_{iL}=1.14 A)	257.51	230.31	257.51*	146.69*	230.31	59.71
ENERGY (L) [mJ]	67.29	60.18	74.36	50.76	60.18	15.6

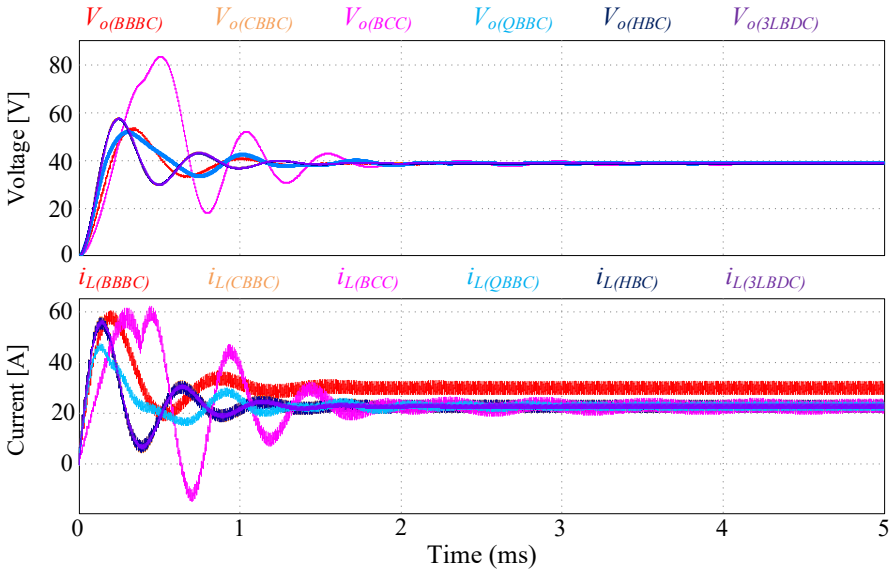


Figure 3.7: Open loop test, comparison of the bidirectional converters.

In Table 7, the current ripple was calculated considering an inductance of 59.7 µH for every converter. A zoom view of the inductor's current in steady state condition is depicted in Figure 3.8, where it is clear that the 3L BDC has the smallest current ripple among the six converters. The BBBC, BCC, CBBC, QBBC, present a high current ripple, 4.93 A for the first BBBC and BCC, and 4.41 A for the CBBC and the QBBC. The 3L BDC converter offers around four times less ripple current than the previous four converters. Moreover, the 3L BDC's current ripple is half of the size of the QBBC.

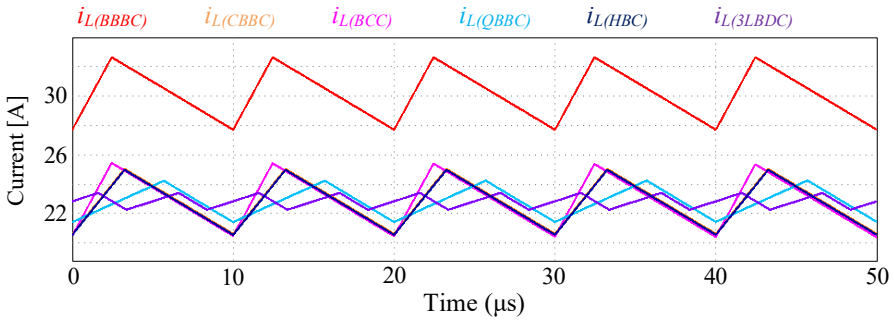


Figure 3.8: Zoom view of the inductor's ripple current of Figure 3.7.

Additionally, the Table mentioned above presents the inductor size if a fixed inductor's current ripple of 1.14 A is considered, then the value of the required inductor is calculated for all the converters. Furthermore, the total energy stored in the inductors is determined because perhaps the number of inductors could be more than one on some converters, the required energy could be equivalent or lower to a single inductance on other topologies. For example, the BCC and the QBBC require two inductors, which could be translated to a large amount of energy. But, the results proved that even though the QBBC uses two inductors, the required energy is less than the required energy by other converters like BBBC, CBB, or the BCC. Still, contrary to the QBBC, the BCC, which also requires two inductors, requires an amount of energy that is actually large.

The comparison Table 8 presents the switching blocking voltage rate, which is a crucial characteristic to consider. Some converters (BBBC, for example) require only two switches, but they must block a large amount of voltage; in contrast, the 3LBDC's four switches only block half of the input voltage. Consequently, a new parameter is introduced to the table, the weight of the converter, which considers the number of switches and the blocking voltage. With the new parameter, there is a fair comparison between the converters. Returning to the previous example, the BBBC has two switches that block, in the worst-case scenario, two times V_i, and then the weight of the converter is four. The case of the 3LBDC is different, perhaps it requires four switches, the blocking voltage is half V_i then the weight of this converter is two, and this weight is equivalent to the HB converter.

Due to its features, the 3L BDC converter resulted in the most promising of the analyzed converters. Thereby, this converter was selected as the BDC converter for this thesis's battery energy storage system stage.

Table 8: Comparison of bidirectional DC-DC converters.

FEATURE	BBBC	CBBC	BCC	QBBC	HBC	3L BDC
POWER LOSSES	AVG	HIGH	LOW	AVG	LOW	AVG
SWITCHES	2	4	2	4	2	4
DIODES	0	0	0	2	0	0
INDUCTORS	1	1	2	2	1	1
CAPACITORS	2	2	3	1	2	3
CURRENT RIPPLE	$\frac{V_i D}{f_{sw} L}$	$\frac{V_i D}{f_{sw} L}(1-D)$	$\frac{V_i D}{f_{sw} L}$	$\frac{V_i D^2}{f_{sw} L}(1-D)$	$\frac{V_i D}{f_{sw} L}(1-D)$	$\frac{(V_i - 2V_o) D}{2 f_{sw} L}$
DUTY CYCLE	$V_o/(V_o+V_i)$	V_o/V_i	$V_o/(V_o+V_i)$	$(V_o/V_i)^{0.5}$	V_o/V_i	V_o/V_i
SWITCH'S B.V.	$V_{in}+V_o$	V_{in}	$V_{in}+V_o$	V_{in}	V_{in}	$0.5V_{in}$
CONV. WEIGHT	4	4	4	6	2	2

B.V. = BLOCKING VOLTAGE. CONVERTER'S WEIGHT = SWITCHES × B.V (V_{in} = 1). * 2 INDUCTORS (L1=L2).

3.2. 3L BDC CONVERTER DESIGN

Compared with other bidirectional converters, the 3L BDC converter's inductor is small; thereby, the dynamic response is improved, making this converter ideal for integrating renewable energy sources based on DC. Additionally, the voltage stress on the power switches is half of the high voltage side, making it suitable for high voltage applications.

3.2.1. OPERATION PRINCIPLE

Figure 3.9 is the electrical circuit of the 3L BDC converter for its analysis. V_H and V_L represent the converter's high and low voltage sides, respectively. A decoupling capacitor is added with the same nomenclature (C_H and C_L) on each side of the converter. L is the only required inductor for the converter, and C_{fly} is the flying capacitor that must be controlled. This converter requires four power switches Q_1-Q_4, where Q_1, Q_4, and Q_2, Q_3 work on complementary configuration, while Q_1, Q_2, and Q_3, Q_4 work under interleave configuration.

The converter works in buck operation mode when the current flows from V_H to V_L. In buck mode, PWM controls Q_1 and Q_2 to regulate the output voltage (V_L). As a result, switches Q_1 and Q_2 act as active switches, while Q_3 and Q_4 are the passive switches working as synchronous rectifiers. Oppositely, as soon as the current flows from V_L to V_H, the BDC converter operates in boost operation mode. In this boost mode, Q_3 and Q_4 are controlled to regulate the output voltage (V_H). In this scenario, the switches Q_3 and Q_4 are the active devices and Q_1 and Q_3 work as passive devices.

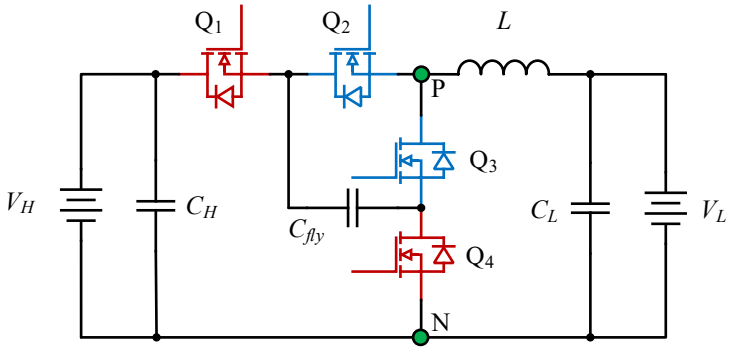


Figure 3.9: 3L BDC converter's operation.

Two duty cycles are defined, D for active switches and D' (D' is complementary to D) for passive switches, where D is defined as $0 \leq D \leq 1$. Additionally, there are two operation modes: $D > 0.5$ and $D \leq 0.5$.

In Figure 3.10, the switching states of the four switches of the BDC converter are drawn, as well as the voltage between the points P and N. If C_{fly} is controlled to be $V_H/2$, then it's clear how the switches always block half of the V_H. For example, consider the interval time from t_0 to t_1 in Figure 3.10. In this interval, V_{PN} is $V_H/2$, as Q_1 is on, then C_{fly}'s positive terminal is connected to V_H. Next, as Q_3 is also on, then the C_{fly}'s negative terminal is connected to the P point; consequently, Q_2, which is turned off, ends up parallel to C_{fly}, then it must block its voltage. Finally, Q_4 is connected to the P, and N points whose value is $V_H/2$ will block that voltage. If a similar analysis is followed in each switching state, it will be noted that all the switches block C_{fly}'s voltage.

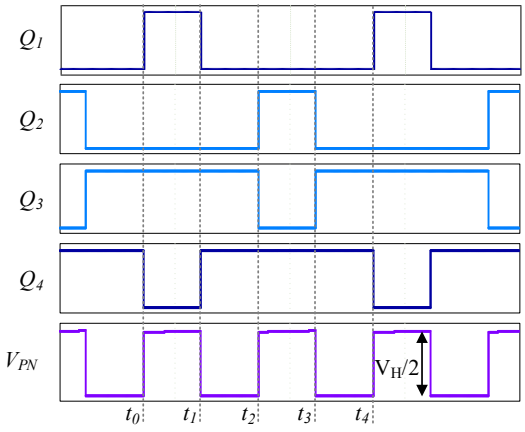


Figure 3.10: Switching states of the 3L BDC converter.

3.2.2. SWITCHING SCHEME

As mentioned previously (Figure 3.10), Q_1 and Q_2 work in interleave mode, then v_{tri1} and v_{tri2} are two triangular waveforms phase-shifted 180° each other, these two carriers are compared against the control signals *a* and *b,* and the output of each comparator generates X_1 and X_2, respectively. When the converter operates in buck mode, Q_1, and Q_2 work as the active switches, then the inputs X_1 and X_2 must drive Q_1 and Q_2. On the contrary, active switches Q_3 and Q_4 must be driven by X_2 and X_1 in boost mode, respectively. Hence, a demultiplexer is needed, which will work as a selector depending if the converter works on boost or buck mode. The timing diagram of the demultiplexer shown in Figure 3.11 is found in Table 9.

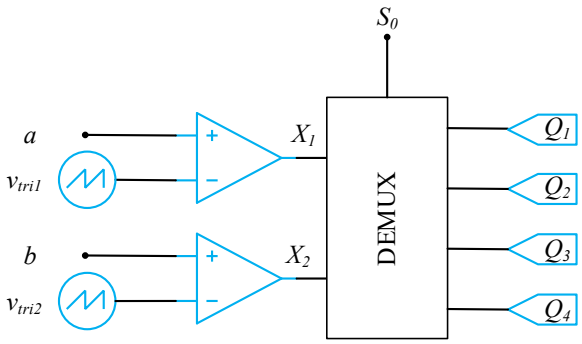


Figure 3.11: Switching scheme.

Table 9: Timing diagram of the demultiplexer.

X_1	0	1	0	1	0	1	0	1	0
X_2	0	0	1	1	0	0	1	1	0
S_0									
Q1	0	1	0	1					0
Q2	0	0	1	1					0
Q3					0	0	1	1	
Q4					0	1	0	1	

3.2.3. VOLTAGE CONVERSION

The power in the 3L BDC converter flows bidirectionally; thus, this converter does not work in discontinuous mode. In voltage reduction mode, V_H is the input voltage, and V_L is the output voltage, then V_L is

$$V_L = DV_H \tag{3.1}$$

Where D is the duty cycle of the active switches, this converter's conversion gain is the same as the classic buck converter. Similarly, during the boost operation mode, V_L is the input voltage, and V_H is the output voltage calculated as follows:

$$V_H = \frac{1}{1-D} V_L \tag{3.2}$$

3.2.4. INDUCTOR DESIGN

As described before, the 3L-BDC converter can work on buck and boost mode; then, the inductor can be calculated either way. The inductor design is calculated in step-down voltage conversion mode to compare this converter with a classical buck converter. Due to there are two operation modes for the duty cycle ($D > 0.5$, and $D \leq 0.5$), it is necessary to calculate the current ripple in both scenarios. Equations (3.3) and (3.4) describe the current ripple for the 3L-BDC converter, and the equation (3.5) defines the current ripple for a classical buck converter.

$$\Delta_{IL} = \frac{(V_H - V_L)(2D-1)T_s}{2L} \tag{3.3}$$

$$\Delta_{IL} = \frac{(V_H - 2V_L)DT_s}{2L} \tag{3.4}$$

$$\Delta_{IL} = \frac{(V_H - V_L)DT_s}{L} \tag{3.5}$$

Xinbo Ruan et al. [50] showed that the maximum ripple current of the inductor of the 3L BDC converter is only one-fourth of the buck converter. In other words, if the ripple currents are equal on both converters, then the inductance size could be down-sized to one-fourth of the buck converter (refers to section 3.1.7 to verify the comparison), which is translated that the 3L-BDC converter has a faster dynamic response. The answer to such a phenomenon is that the voltage on the inductor has lower high-frequency content than the buck converter. The ripple frequency of the voltage mentioned above is twice the switching frequency. This is a similar behavior

that multilevel inverters present, where the switching frequency is effectively doubled compared with 2L inverters.

In order to design the sizing of the converter's inductance, the equation (3.6) can be considered because the 3L BDC converter is an extension of the buck converter, where the special considerations about the current ripple were explained before.

$$L = \frac{(V_H - 2V_L)D}{2\Delta_{IL} f_{sw}} \tag{3.6}$$

3.2.5. FLYING CAPACITOR DESIGN

The continuous charging and discharging of the flying capacitor (C_{fly}) produces its voltage has a ripple. This capacitor will also be calculated in buck mode as it was done with the inductor. T_{fly} is the charging time of the flying capacitor within one switching cycle. The charging current of C_{fly} is:

$$I_{Cfly} = \frac{P_o}{V_L} \tag{3.7}$$

Then, C_{fly} can be calculated as follows:

$$C_{fly} = \frac{I_{Cfly} T_{Cfly}}{\Delta V_{Cfly}} \tag{3.8}$$

Where ΔV_{Cfly} is the ripple voltage, a parameter defined by the converter's designer. Finally, T_{Cfly} is defined by:

$$T_{Cfly} = \begin{cases} DT_{sw} & 0 < D \leq 0.5 \\ (1-D)T_{sw} & 0.5 \leq D \leq 1 \end{cases} \tag{3.9}$$

Simulation results regarding the behavior of the flying capacitor and its ripple voltage are found in section 3.3.

3.2.6. SIZING OF THE ENERGY STORAGE SYSTEM

To verify the converter's operation, first needed to size the 3L-BDC converter. The objective is to design a 3L-BDC converter that can discharge and charge the lithium-ion battery taking or supplying energy bidirectionally towards a DC BUS.

The BESS is designed as part of a scaled-down prototype that was briefly introduced in chapter 1. The general parameters of the converter mentioned above, seen for now

as a black box, are listed next. The RMS line-to-line output voltage is 400/3 V, the DC link is 120 V, and the rated output power is 3 kW. Therefore, the battery pack must be able to supply the rated power, and the 3LBDC converter should handle the same amount of power.

3.2.6.1 Sizing of the battery pack

Previous to designing the 3L-BDC converter, the battery pack must be developed. The design will consider the battery's actual parameters for a scaled-down prototype. In this case, a commercial 48.1 V battery pack will be designed, rated at 3 kW. This battery pack considered for all the simulations is integrated with model 18650 single-cell batteries produced by Sanyo Electric [51]. Each battery cell has a nominal voltage of 3.7 V, a minimum capacity of 3350 mAh, a charging current of 3.35 A (1 C) per cell, and a maximum continuous discharge current (MCDC) rate of 10 A. These and other important parameters are listed in Table 10.

Table 10: Battery parameters.

Parameter	Variable	Value
Model Name		NCR8650GA
Nominal voltage	V_{cell}	3.7 V
End voltage	V_{end}	2.5 V
End voltage recommended	V_{endr}	3.0 V
Fully charged voltage	V_{full}	4.2 V
Rated capacity	Q	3300 mAh
Capacity (minimum)	C	3350 mAh
Continuous discharge current	I_{max}	10 A
Charging current	I_{ch}	0.5 C
Maximum charging current	I_{chmax}	1 C
Pre-charging current	I_{pre}	0.1 C
Cutoff current	I_{cut}	0.1 C

To supply 3 kW, the continuous discharge current in the battery pack is

$$I_{pack} = \frac{3\,kW}{48.1V} = 62.37\,A \tag{3.10}$$

From [51] it is known that the maximum continuous current is 10 A, then to satisfy this restriction, it's necessary to share the current between several batteries. The number of parallel batteries (N_p) can be obtained by dividing the current battery pack over the MCDC; this number must be an integer.

$$N_p = \frac{I_{pack}}{MCDC} = 6.23 \rightarrow 7 \tag{3.11}$$

From the previous equation, seven batteries will be required to supply the necessary current. Now, the nominal battery current in discharge mode can be calculated as follows:

$$I_{cell} = \frac{I_{pack}}{N_p} = 8.91A \tag{3.12}$$

The maximum charging current is

$$I_{ch\max} = 1C \cdot N_p = 23.45A \tag{3.13}$$

The number of series-connected batteries is

$$N_s = \frac{V_{pack}}{V_{cell}} = 13 \tag{3.14}$$

The backup time for the rated power is

$$t_{backup} = \frac{Wh}{W} = \frac{V_{pack} Q N_p}{\sqrt{3} V_o I_o} = \frac{1.11kWh}{3kW} = 0.37h \tag{3.15}$$

3.2.6.2 Sizing of the 3L-BDC converter

This section performs the sizing of the 3L-BDC converter in buck mode. This means that the input voltage is V_H = 120.0 V (DC BUS), the output voltage is V_L = 39.0 V (recommended minimum battery pack voltage to expand lifetime), and the maximum allowed charging current in the battery pack is 23.45 A. Considering the last value and that the ripple current is 5%, the battery charging current is calculated as follows:

$$I_{ch} = I_{ch\max} - \frac{\Delta I_{ch}}{2} = 22.86\,A \tag{3.16}$$

Due to batteries being so sensitive, the maximum parameters should never be overpassed. If the $I_{ch\max}$ is used as the battery charging current, then the current ripple will overpass the maximum allowed current for the charging process, and this is not desirable. Therefore, the correct way to calculate the battery charging current is considering that the maximum allowed current is equal to the battery current plus the ripple current.

The voltage ripple in the battery pack is set to 2.5 % (136.5 mV) of the battery pack voltage. This strict voltage ripple is as well selected due to security reasons. The full charged voltage for a cell is 4.20 V, and the datasheet allows 30 mV of overcharged case scenario. Considering the battery pack voltage, the overcharged voltage range goes to $N_s \times 30$ mV = 390 mV.

The ripple current on the battery pack in charging mode is

$$\Delta I_{ch} = I_{ch} \cdot 5\% = 1.14\,A \tag{3.17}$$

The duty cycle can be calculated as:

$$D = \frac{V_L}{V_H} = \frac{V_{pack}}{V_{bus}} = 0.325 \tag{3.18}$$

For the inductor size, a switching frequency of 100 kHz is considered (Table 6), and the equation (3.6) is recalled:

$$L = \frac{\left(V_H - 2V_L\right)D}{2\Delta I_L f_{sw}} = 59.70\,\mu H \tag{3.19}$$

The L_V capacitor (C_L) is designed as follows:

$$C_L = \frac{\Delta I_L}{8 f_{sw} \Delta V_L} = 10.47\,\mu F \tag{3.20}$$

Finally, the flying capacitor is obtained from the equation (3.8)

$$C_{fly} = \frac{I_{Cfly} T_{Cfly}}{\Delta V_{Cfly}} = 17.33\,\mu F \tag{3.21}$$

3.2.7. MODELING OF THE 3LBDC CONVERTER

The main consideration that must be taken into account prior to starting the modeling is that the voltage of the flying capacitor is well regulated to half of the input voltage

for buck mode or half of the output voltage in boost mode. From [46, 50, 52] it is known that the 3LBDC converter can be modeled as a 2LBDC converter; hence, the buck converter's model is a good option. The primary consideration to be aware of using the buck converter model is that the 3LBDC converter's switching frequency is equivalent to two times the switching frequency of the 2LBDC converter.

The modeling is based on the small-signal approach. The present model (Figure 3.12) considers the parasitic resistances in the passive elements. When the switch Q is turned on, the duty cycle is *d*; on the contrary, when Q is turned off, the duty cycle is *1−d*. Then, the circuit must be analyzed considering both states.

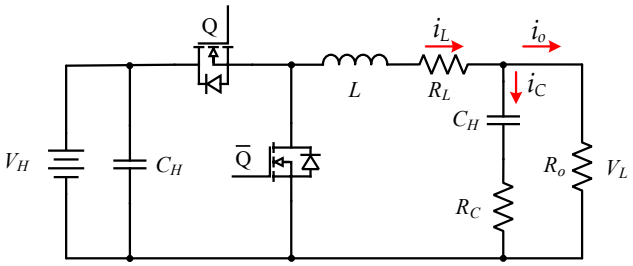


Figure 3.12: Circuit diagram of a 2L DC-DC converter.

Applying the Kirchhoff laws to the circuit when Q is turned on, and considering that the inductance and the capacitances are the state variables, while the output variable is the output voltage, the differential equations are derived as follows

$$\begin{aligned} L\frac{di_L}{dt} &= v_H - v_L - R_L i_L \\ C_L\frac{dv_C}{dt} &= i_L - i_o \\ v_L &= v_C + R_C\left(i_L - i_o\right) \end{aligned} \tag{3.22}$$

The differential equations when Q is turned off are the next ones:

$$\begin{aligned} L\frac{di_L}{dt} &= -v_L - R_L i_L \\ C_L\frac{dv_C}{dt} &= i_L - i_o \\ v_L &= v_C + R_C\left(i_L - i_o\right) \end{aligned} \tag{3.23}$$

The state variables are continuous in time; hence the definition of those equations over a switching cycle is as follows

$$
\begin{aligned}
L\frac{di_L}{dt} &= dv_H - v_L - R_L i_L \\
C_L\frac{dv_C}{dt} &= i_L - i_o \\
v_L &= v_C + R_C\left(i_L - i_o\right)
\end{aligned}
\tag{3.24}
$$

Due to equation (3.24) has the term dv_H the model is not linear and must be linearized. The procedure is well known and can be found in [53-55] is based on the work made by Middlebrook, Cúk, et al.; it is a state-space averaging technique that generates a linear model for small AC signals, taking into account a linearization around a steady state DC operating point. The transfer function control input to output voltage without considering the inductor's parasitic resistance is obtained:

$$
G_p(s) = \frac{\tilde{v}_L(s)}{\tilde{d}(s)} = \frac{V_H\left(1 + sR_C C_L\right)}{s^2 LC_L\left(\frac{R_C}{R}+1\right) + s\left(\frac{L}{R} + R_C C_L\right) + 1} \tag{3.25}
$$

Where $\tilde{v}_L = v_L - V_L$ and $\tilde{d} = d - D$. As can be seen, each variable is integrated by a DC term and a small AC term.

3.2.8. CONTROL SCHEME

3.2.8.1 Considerations

- Interleaving switching method: The switches Q_1, Q_2, and Q_3, Q_4 will operate in interleaving mode to increase the switching frequency effectively.
- Bidirectional power flow: to achieve this feature, the currents and voltages of V_H and V_L must be fully controllable. Thereby, the V_H, V_L, and V_{Cfly} must be sensed as well as the inductor current I_L.
- The Flying capacitor's voltage must be regulated: In order for the switches in the converter to block half of V_H all the time, the flying capacitor's voltage must be controlled to be $V_H/2$

3.2.8.2 Frequency-domain voltage-mode control

Figure 3.13 presents the control system, where $G_v(s)$ represents the transfer function of the voltage control law, $G_{PWM}(s)$ the pulse-width modulator, and $G_p(s)$ describes the plant transfer function. The transfer functions mentioned above are described below

$$
G_{PWM}(s) = \frac{1}{V_{carrier}} \tag{3.26}
$$

$$G_v(s) = K_p\left(1+\frac{K_i}{s}\right) \tag{3.27}$$

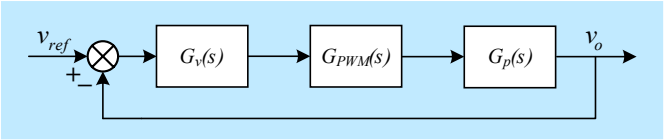


Figure 3.13: Control loop's block diagram of the 2L DC-DC converter.

From Figure 3.13, the loop gain transfer function can be derived as

$$T_v(s) = G_v(s)G_{PWM}(s)G_p(s) \tag{3.28}$$

The bode plot of the $G_p(s)$ is shown in Figure 3.14. Its crossover frequency is found at 452 krad/s; however, the switching frequency is at 628.31 krad/s. On the other hand, the open loop transfer function should cross the 0 dB one decade below the switching frequency; in other words, w_c should cross at 62.83 krad/s; therefore, a controller is necessary to satisfy this condition.

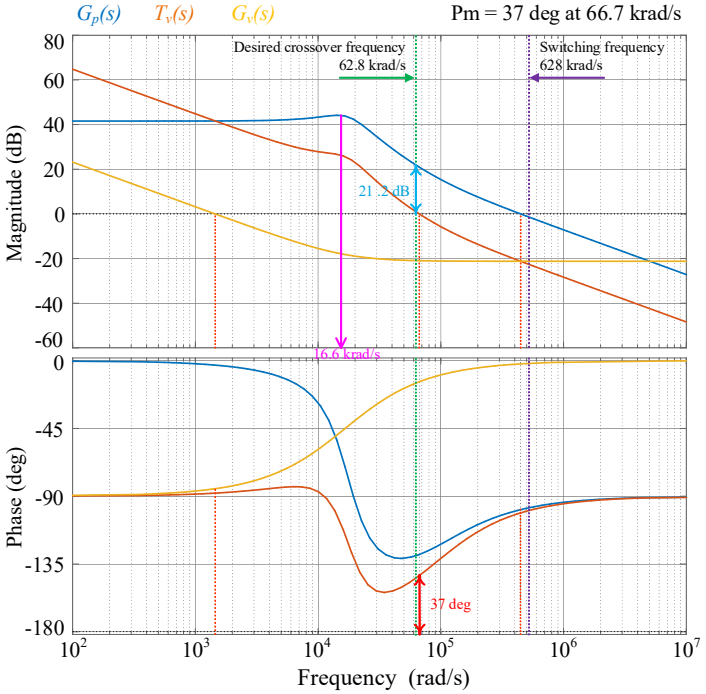


Figure 3.14: Bode plot of the most important transfer functions, Gp(s), Tv(s), Gv(s).

The control to output's gain at w_c = 62.83 krad/s is 21.9 dB, then the PI's proportional gain must be K_p = −21.9 dB = 0.080. The integral gain is associated with the corner frequency of $G_p(s)$; then, K_I = 15.2 krad/s.

Figure 3.14 also presents the bode plot of the loop gain. As seen in the orange trace, the actual crossover frequency (66.71 krad/s) is around the desired crossover frequency (62.83 krad/s). At the current w_c, the phase margin is 37 deg. Figure 3.15 presents the bode plot of the closed-loop transfer functions of the equations (3.29) and (3.30). Figure 3.16 shows the step response for the same transfer functions. The transfer function $G_{p\_cl}(s)$ presents a fast rise time but has an error on steady-state. The tune strategy so far presented is a starting point for the tuning process.

$$G_{p\_cl}(s) = \frac{G_p(s)}{1 + G_p(s)} \tag{3.29}$$

$$G_{CL}(s) = \frac{T_v(s)}{1 + T_v(s)} \tag{3.30}$$

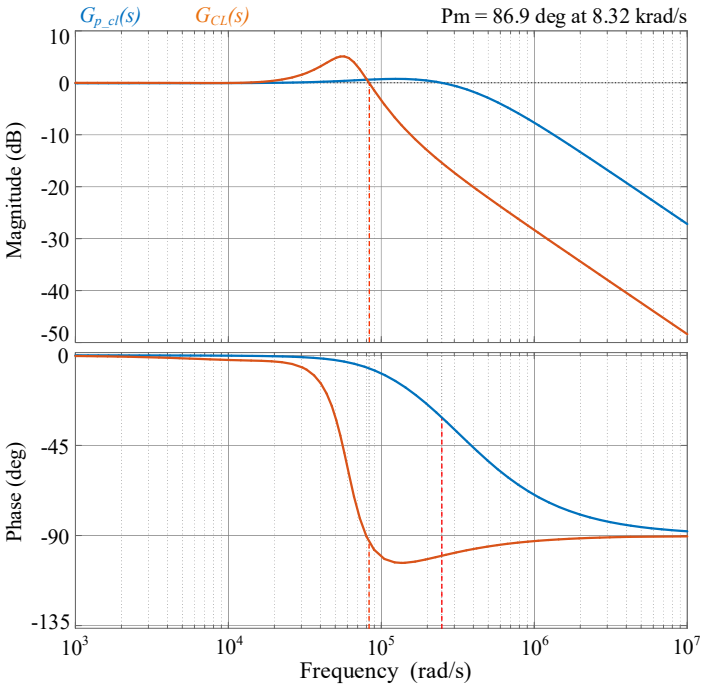


Figure 3.15: Bode plots of closed-loop transfer functions $G_{CL}(s)$ and $G_{p\_cl}(s)$.

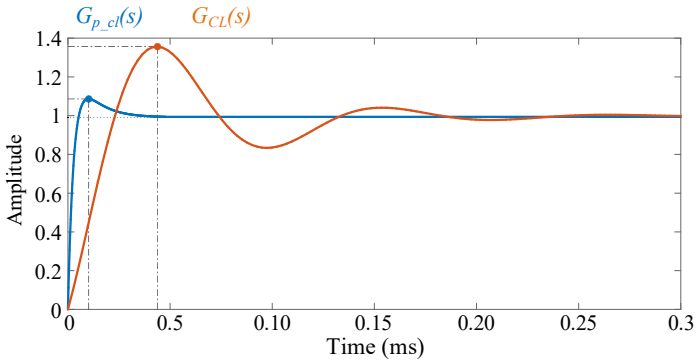


Figure 3.16: Step response of the transfer functions presented in the previous figure.

3.2.8.3 Flying capacitor voltage control strategy

If the duration of the turn-on and turn-off process of the set of switches Q_1, Q_4, and Q_2, Q_3 are equal, and both sets of switches are the same (from the electrical point of view), then the voltage on the flying capacitor will be half of the V_H voltage, i.e., $V_{Cfly}=V_H/2$. Then, under such circumstances, the switches' blocking voltage is the same for the four switches and equal to the V_{Cfly}. But, in practice, minor differences make it improbable that the switches block the same voltage. Those differences could be related to the PWM generators, the driver devices, and the switches themselves; therefore, there is a slight difference between the switches' duty cycles, which causes the charging and discharging current rate on the flying capacitor to be different within a switching cycle.

A floating sensor must acquire the flying capacitor voltage (V_{Cfly}). The sensor gains must be chosen as follows, for V_{Cfly}, the gain $k = K_H$, and for V_H, the gain must be $k = K_H/2$. The sign of k (+ or −) changes depending on if the current I_L is positive or negative. There is no restriction for the current's gain. The control scheme is in Figure 3.17; it can be seen that it is integrated by two regulators, a current controller and a flying capacitor voltage controller, $G_{C1}(s)$ and $G_{C2}(s)$, respectively. The Proportional + Integral (PI) compensators are implemented in both controllers. The addition of $u_i + u_v$ results in a, then a is compared with the triangular waveform v_{tri1} of Figure 3.11. Similarly, $-u_v + u_i$ equals b, and this signal then is compared with v_{tri2}.

If the converter works in buck mode and the duty cycle of Q_1 is bigger than Q_2, then the flying capacitor's voltage will be greater than half of the input voltage; this is evaluated by means of the bottom adder. The output of the adder is the error signal e_v which will be compensated by the PI controller ($G_{C2}(s)$), and then u_v is obtained. The negative of the control signal u_v, plus u_i is b, as was explained before. Continuing, let's consider that $V_{Cfly} > V_H/2$, this implies that $-u_v > 0$, this will decrease a; thereby, the duty cycle on Q_1 is reduced as well. On the contrary, if $u_v < 0$, b will increase, and

consequently, the duty cycle on Q_2 also increase. Tweaking the duty cycles will reduce the voltage of the flying capacitor, and it will end up with V_{Cfly} reaching $V_H/2$. Now, consider that $V_{Cfly} < V_H/2$, this will make that $u_v > 0$, which will increase a; therefore, the duty cycle on Q_2 increases. In case that $-u_v < 0$, b decreases; as a result, the duty cycle on Q_2 will decrease as well; subsequently, V_{Cfly} will increase until it reaches $V_H/2$. A similar study can be performed for the boost case.

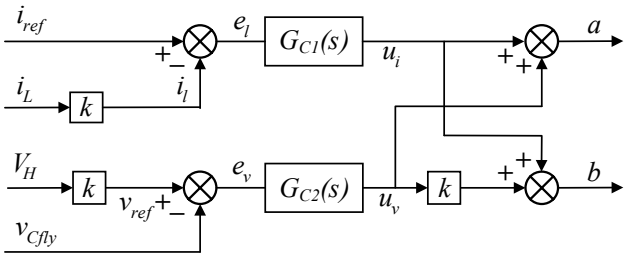


Figure 3.17: 3L-BDC control structure.

3.3. 3L-BDC SIMULATION

Once the 3L-BDC converter is sized, its performance is analyzed through a simulation. The input and the output voltage sources are considered ideals in this simulation. The main parameters used in this simulation are listed in Table 11.

Table 11: 3L-BDC simulation parameters.

Parameter	Variable	Value
Input voltage	V_H	120 V
Output voltage	V_L	39 V
Output current	I_{ch}	22.84 A
Inductor	L	59.70 µH
Switching frequency	f_{sw}	100 kHz
Flying capacitor	C_{fly}	17.33 µF
Output capacitor	C_L	10.47 µF
Current proportional gain	K_c	1
Current time constant	Ti_c	100 µ
Voltage proportional gain	K_v	0.3
Voltage time constant	Ti_v	100 m

Figure 3.18 is organized into three sections and two columns. The two columns are the full view (left side) and a zoomed view (right side); the zoom view presents the details of the high-frequency waveforms. The voltage, current, and control signal integrate the three sections.

The first section presents the voltage in the low voltage side (V_L) and the voltage in the flying capacitor (v_{Cfly}). Due to the ideality of the output voltage source, its waveform is represented by a plain line; on the contrary, the flying capacitor voltage presents a dynamic similar to a first-order system. The $G_{c2}(s)$ control objective is to regulate the voltage on v_{Cfly} to be half of V_H, which is fully accomplished; thereby, the four switches of the 3L-BDC converter will block only this voltage instead of blocking V_H. On the zoomed view, the voltage ripple is shown; the voltage ripple in the simulation is 4.27 V.

The following section displays the inductor current. This current is regulated by $G_{c1}(s)$, which reference is set by the equation (3.16). The ripple current on the inductor is 1.15 A. On the zoom view, it is seen that the current ripple is twice the switching frequency. This phenomenon was explained before, but this is due to the converter's switches working on interleave operation mode.

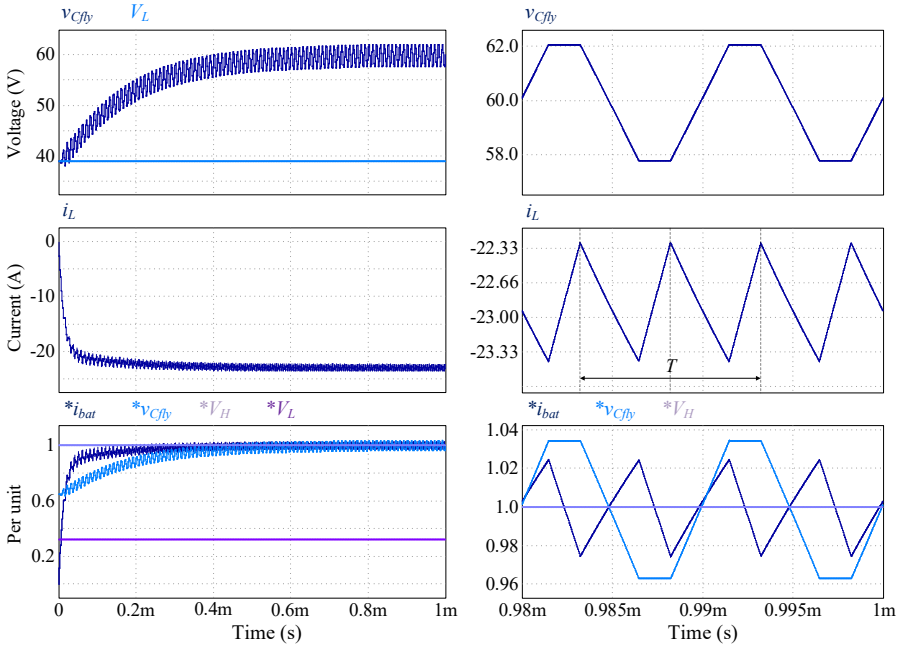


Figure 3.18: Simulation results of the 3L-BDC converter on buck operation.

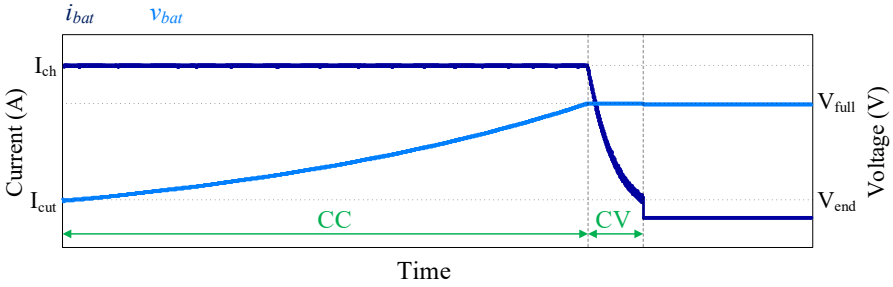


Figure 3.19: Battery charging process.

Finally, on the voltage section are four signals (i_{bat}, v_{Cfly}, $V_{H,}$ and V_L) marked with an asterisk (*); this stands for measurements taken by the sensor. The sensor's gains will produce per unit results. For example, consider the gain of the high voltage side sensor to be 1/120; if the V_H = 120 V, then the output signal of the voltage sensor is 1. Through this figure, it is more evident how the voltage on the flying capacitor and the current on the inductor gets controlled.

3.4. CONTROL STRATEGY TO CHARGE A LI-ION BATTERY

The Li-ion batteries are naturally sensitive to overvoltage and undervoltage circumstances. If batteries are overcharged (when the SOC of a battery is taken beyond the design limit), the battery's lifetime is compromised, and it can trigger a potential vent, "vent is a weak point in the device that allows an opening to occur upon conditions that might lead to or indicate the occurrence of thermal runaway" [56], that can be catastrophic. In the same line, a deep over discharge can cause, in some cases, gassing and a thermal runaway [57]. On the contrary, undercharging a battery could lead to poor performance from the capacity point of view [58]. For example, if the fully charged voltage is considered 100 %, and the battery is only charged to 98,8 % of the charged voltage, then the remaining 1.2 % represents 9 % of capacity loss.

In order to charge a battery properly, the power electronic converter typically starts by supplying a regulated constant current through the battery; this process is commonly finalized when the battery reaches the fully charged voltage limit of the battery found in the datasheet of each battery. From this point, the power converter must provide regulated constant voltage while the current through the battery starts falling; this process will end once the battery current falls to a defined limit called cutoff current limit. The described charging method Figure 3.19 is known as constant-current (CC), constant voltage (CV) charging method (CC-CV) [59][60][61][62]. This process commonly considers two stages, CC and CV, but there is a preliminary stage within the CC under specific circumstances. The preliminary stage is activated when the battery voltage is below the end voltage limit (2.5 V); in such conditions, the power converter injects no more than the pre-charging current (0.33 A).

The 3L-BDC converter implements the mentioned battery charging process. To implement the strategy depicted in Figure 3.20, it is required to sense the battery voltage and current. Additionally, two control laws are needed, $G_{CC}(s)$ for the constant current stage and $G_{CV}(s)$ for the constant voltage stage. Both control laws are PI controllers. The battery charging algorithm, now called BCA (Figure 3.21), decides which control law is active or inactive. The complete control structure that allows operating the 3L bidirectional converter is depicted in Figure 3.22; this control structure works for charging the battery from the PV system or the grid and discharging the battery when it is supplying power to the grid. A simulation is performed to verify if the 3L-BDC is working correctly as a battery charger. The simulation parameters and some considerations are listed in Table 12; other simulation parameters keep the same values as in previous simulations. During this simulation, the battery model explained in section 2.2.2 is used.

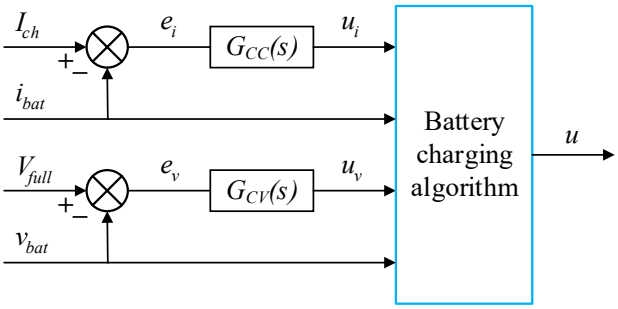


Figure 3.20: Control scheme for the battery charging process.

Table 12: Simulation parameters for the battery charging process.

Parameter	Variable	Value
Fully charged voltage	V_{full}	42.0 V
Maximum charging current	I_{chmax}	22.86 A
Cutoff current	I_{cut}	20.00 A
Current proportional gain	K_c	0.02
Current time constant	Ti_c	0.036
Voltage proportional gain	K_v	0.33
Voltage time constant	Ti_v	0.16

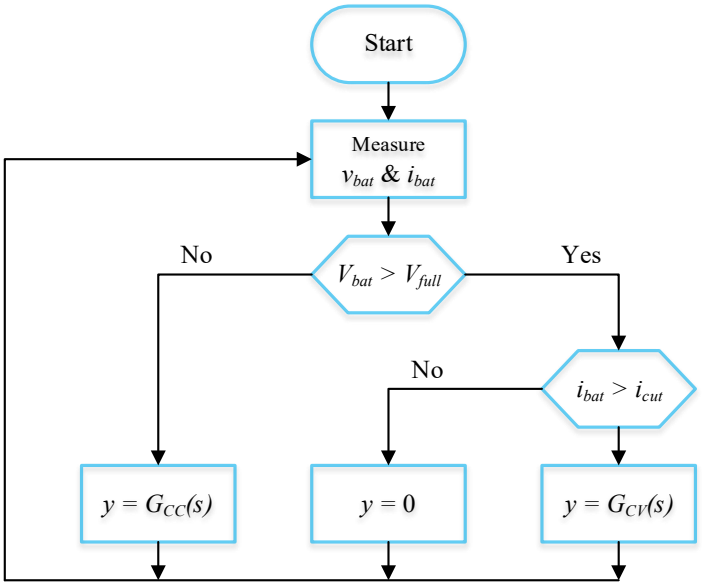


Figure 3.21: Control law selector for the battery charging process.

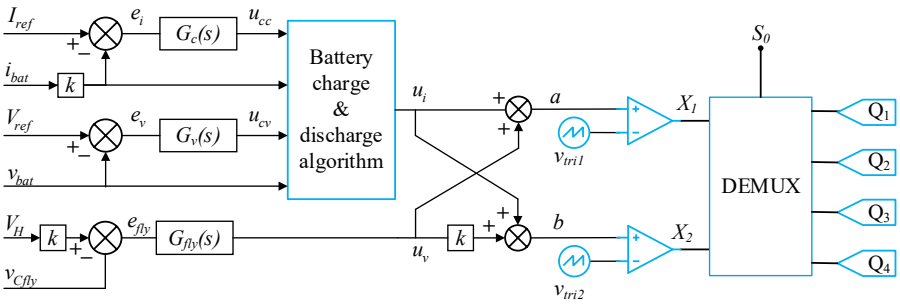


Figure 3.22: Complete control structure that operates the 3L bidirectional converter.

For this simulation, the following considerations are taken into account. Due to the converter's switching frequency being 100 kHz, trying to charge the battery under a simulation environment will take a lot of time. The simulation ratio is approximately 1000:1, depending on the processor speed. Therefore, to simulate the charging process, some parameters were modified. The initial battery voltage is 39.5 V, the fully charged voltage is 42 V, and the cutoff current is 20 A. Under these circumstances, the battery charging process takes one second of simulation time.

Figure 3.23 shows the battery charging simulation. There are three groups of waveforms: battery current, battery voltage, and control signals. The charging process method starts with selecting the controller, CC, or CV. The BCA selects the constant

current method (CC signal is active while CV is in idle mode) because the battery voltage is below 42 V, then the 3L-BDC converter injects 22.86 A into the battery pack until the battery pack voltage reaches the fully charged voltage operation point at $t = 0.42\ s$. From this point, the BCA selects the constant voltage controller (CV signal turns active while CC enters to idle mode), and the power converter regulates its output to 42 V until the charging current falls below the cutoff current limit of 20 A at $t = 0.90\ s$. At this point, the BCA stops the charging process, and the battery is fully charged. The control signal waveforms show when each stage starts and ends and the actual output controller signal, *u(t)*. Here, it is more evident that *u(t)* has a more significant ripple during the CC stage than when the BCA selects the CV controller, whose output is smooth.

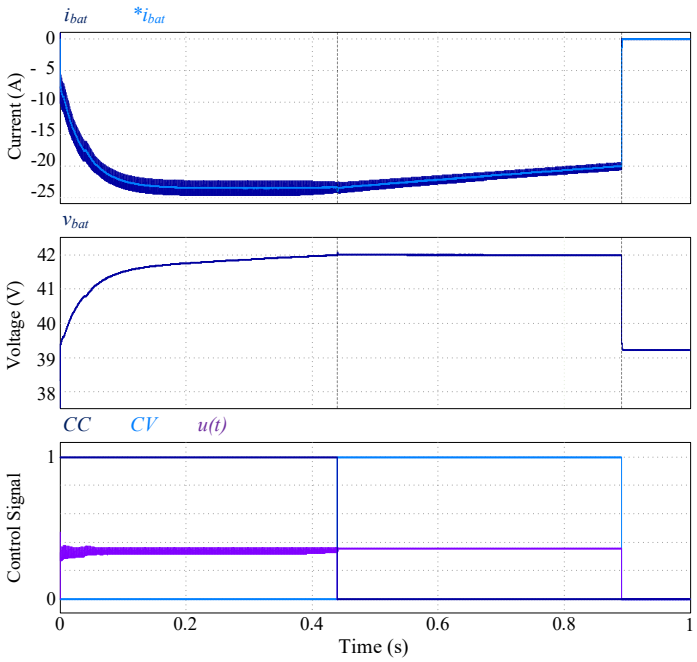


Figure 3.23: Simulation of the 3L-BDC converter charging a battery pack.

3.5. PV SYSTEM WITH 3L-BDC CONVERTER

The converter has been tested as a BESS successfully. In this section, the converter will work as a boost converter for a PV application. The converter's design is kept as in section 3.2.6.2. The PV system is integrated with four PV modules of 250 W each. This module is the same as used in section 2.1.1. The configuration of the PV modules is 2S2P (two in series, two in parallel), which produces an output power of 1000 W under 1000 W/m^2. The PV system will supply energy for a 1000 W resistive load. The power converter must perform MPPT while keeping the flying capacitor regulated to

half the output voltage. The MPPT algorithm implemented in the 3L-BDC converter is the incremental conductance.

Some considerations were taken into account previously to do the simulation. From chapter 2, it is known that the perturbation step for the MPPT algorithm is in the hundred-hertz range. But if this perturbation period is used on the simulation, the simulation run time will take a considerable time because the converter is switching at 100 kHz, and the simulation step is 100 ns. To reduce the simulation time, the perturbation frequency for the MPPT algorithm is set to 3000 Hz, while the step size of the perturbation (Δ_D) is 0.01, which represents 1 % of the duty cycle.

The simulation results are in Figure 3.24. The figure is divided into four sections, powers (available power vs. harvested power), converter's duty cycle, current on the PV array, and different voltages (on the PV array, load, and flying capacitor). During the simulation, four irradiance levels are considered 600, 800, 500, and 1000 W/m^2; ramp functions are implemented between irradiance changes, which tries to emulate a cloud covering the PV plant. This irradiance profile will test that the converter plus the MPPT algorithm works correctly.

The first section of the figure helps visualize if the power converter injects all the available power into the load. $P_{available}$ is the available power on the PV arrays, whereas P_{pv} is the actual harvested PV power. As seen in the figure, there are three ramps; the first one starts at t = 15 ms ($P_{available}$ = 600 W/m^2) and ends 10 ms later ($P_{available}$ = 800 W/m^2), the second ramp begins at t = 40 ms and ends at t = 55 ms; finally, the third ramp is found between $70 < t < 85$ ms.

The duty cycle section noted that the algorithm speed depends on the perturbation frequency and the perturbation step size. Analyzing the waveform, it can be pointed out that the algorithm keeps the perturbation around the MPP (D ± ΔD) once it reaches the MPP; this is normal behavior. Moreover, an erratic behavior during the slopes is noted, especially in the positive ones. The duty cycle presents a behavior like an oscillation that disappears as soon as the slope ends.

The flying capacitor voltage is always well regulated to half of the output voltage, which is ideal, so the converter's switches breaking voltage rate can be reduced. V_H and v_{Cfly} practically do not present overshoots due to the smooth change of P_{pv}. The output voltage is not always constant but reaches the steady-state operation after each irradiance step. The output voltage is not constant because the converter is operating as a current source that provides all the available power to the load. The voltage on the PV arrays varies around the V(MPPT). The steady-state value of the three voltages (V_H, v_{pv}, v_{Cfly}) in each of the four irradiance levels (600, 800, 500, and 1000 W/m^2) are listed next: at 600 W/m^2 the voltages are 91.00 V, 59.07 V, 45.10V in that order. At 800 W/m^2 the values are 106.44 V, 59.82 V, and 53.10 V, respectively. At an irradiance level of 500 W/m^2 the voltages are 83.01 V, 58.38 V, and 41.65 V

correspondingly. Finally, at 1000 W/m^2 the voltage values are 119.70 V, 61.16 V, and 59.94 V, in the same order.

Finally, the current of the PV module is depicted in the last section of the figure. Here the effect of the perturbation step is more evident. The current's four steady state operation points for the four irradiance levels are 9.81A, 13.15A, 8.19A, and 16.30 A, in the order mentioned earlier. In conclusion, the simulation results showed that the converter works appropriately according to the design parameters.

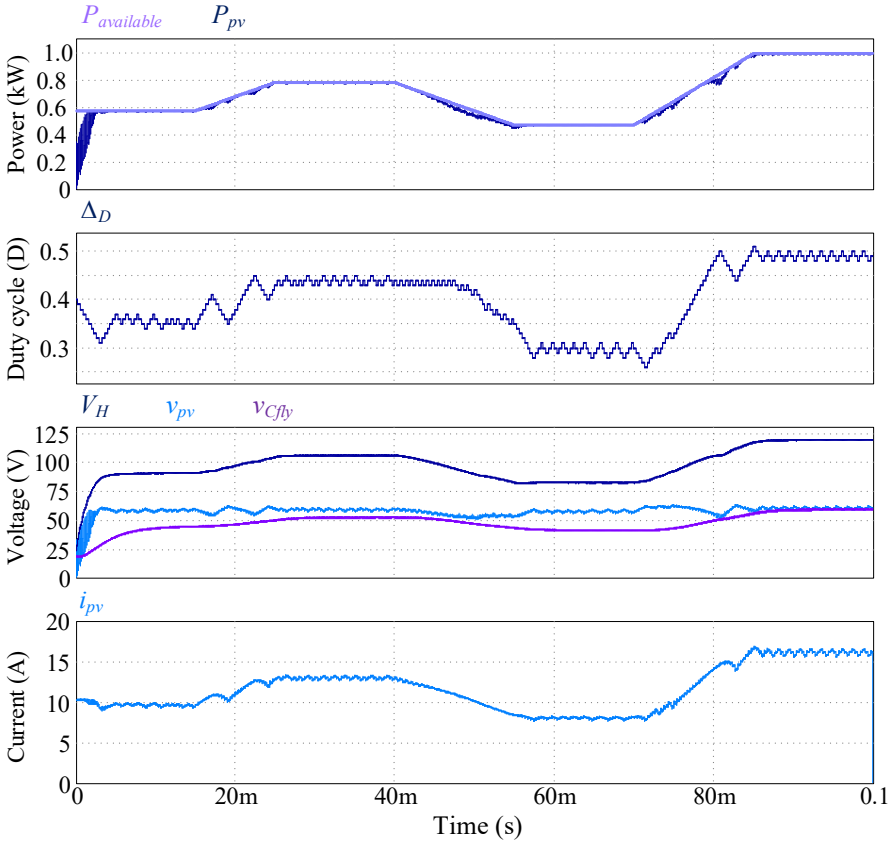


Figure 3.24: 3L-BDC converter working as an MPPT controller.

3.6. PV SYSTEM WITH BESS: 3L-BDC CONVERTER

In this section, PV and BES systems will work together to supply power to a resistive load. The converter parameters for the BESS's 3L-BDC converter are the same as in sections 3.2.6.1, and the considerations for this simulation are also kept. The PV arrays have the following configuration two modules in series (2S) and six modules in

parallel (6P); therefore, the PV arrays can provide to the load at a maximum of 3 kW. The difference in comparison with the previous simulations is that employing the BESS, the voltage on the load (V_H) will be regulated to 120 V during the entire simulation, perhaps any perturbation on solar irradiance. The control objectives of this simulation are to extract the available power on the PV arrays, regulate V_H, keep the flying capacitor regulated to $V_H/2$, and supply constant power to the load.

The simulation results are shown in Figure 3.25 and are grouped into four sections, irradiance, currents, voltages, and powers. The irradiance profile is depicted in the top section, starts from 0 W/m^2, then at $t = 20$ ms there is an increase in the irradiance level, shaped as a slope from 0 to 750 W/m^2 with a duration of 10 ms. The subsequent changes in the irradiance levels are given as step changes from 750 to 500 W/m^2, and from 500 to 1000 W/m^2 at 50, 75 ms, respectively. The BES system starts working first from $t = 0$. It is in charge of generating the regulated voltage on the load (V_H) to 120 V. Because there is no PV generation yet (see $P_{available}$ t = 0 to t = 20 ms), the BES supplies all the power to the load, and the current reaches 87.37 A. The voltage on the load smoothly goes to 120 V at t = 15 ms; the same behavior is shared by the flying capacitor, which reaches its reference at 7.5 ms. The battery pack's voltage falls to 34.29 V due to the high current this is providing to the load.

At $t = 20$ ms, the PV system starts working, but as of t = 30 ms it provides the 2250 W (P_{pv}) to the load while BESS provides the rest (P_{bat} = 750 W); thereby, the loads dissipate P_{load} = 3000 W in total. Because the MPPT algorithm depends on the perturbation frequency (Δ_D), it takes time to increase the power from the previous irradiance level to the new one. The current that the battery is supplying falls from 87.37 A to 21.30 A; consequently, the battery pack voltage increases to 37.33 V. The flying capacitor voltage hardly suffers a modification. In contrast, the high voltage at the transition time presents a small perturbation that last 9 ms; this settling time could be less, but the MPPT algorithm is following the irradiance level ramp. The PV voltage reaches the V(mpp) at $t = 31$ ms. In this waveform, the perturbation effect is more pronounced; the MPPT algorithm performs a perturbation each 500 us; therefore, the voltage continuously switches between three levels, Vmpp, $+\Delta v_{pv}$, and $-\Delta v_{pv}$ where Δv_{pv} is not constant and depends on the current level.

Other irradiance perturbation occurs at $t = 50$ ms. In this case, the irradiance falls to 500 w/m^{2,} which produces that the P_{pv} and P_{bat} are 1433.62 W and 1566.59 W respectively, while the P_{load} is 3000 W. Voltages hardly change their values; $v_{bat,}$ for example, reduces its amplitude due to the battery pack is injecting more current; this behavior is exactly what a good mathematical battery model should represent. V_H and v_{Cfly} remain at 120 V and 60 V, respectively, with a small perturbation at irradiance change.

Finally, at $t = 75$ ms, the last change in irradiance level happens. Here, the solar irradiance jumps from 500 W/m^2 to 1000 W/m$_2$. This produces that the PV system

generates all the power that the load requires, then the P_{bat} drops to zero; in consequence, the battery voltage rises from 36.31 V to 38.27 V. The PV array current is 48.90 A, while the battery current is practically zero. Other variables like V_H and v_{Cfly} remain almost unchanged, perhaps the perturbations.

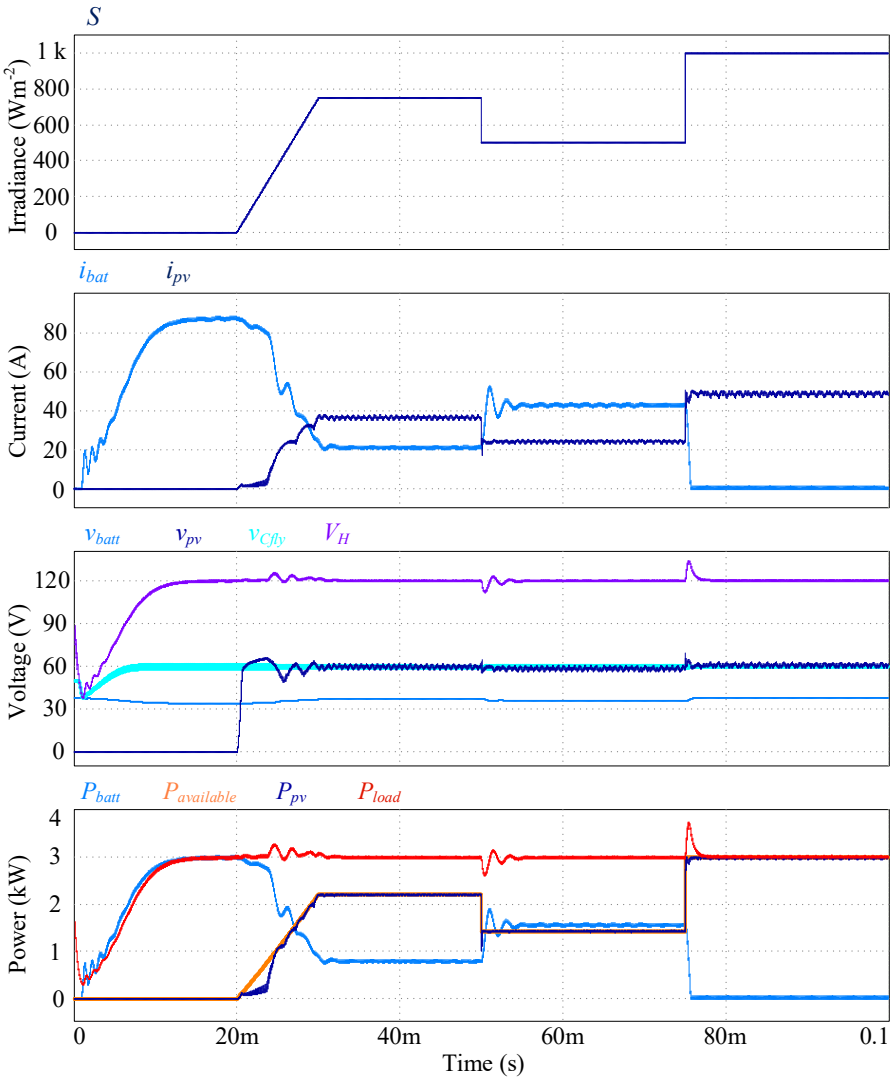


Figure 3.25: Simulations results for PV + BES systems.

In conclusion, this chapter has shown how the 3L-BDC converter operates under different circumstances, including buck or boost operation mode; moreover, the converter's design was analyzed, and finally, study cases where the converter works along with PV and BES systems.

CHAPTER 4. ANALYSIS AND DESIGN OF A CASCADED DC-AC-AC CONVERTER WITH AC-LINK

The fall in prices and the growth of photovoltaics in the last years have required technologies and innovations in power electronic converters to connect large-scale PV power plants to the grid. Nowadays, the most widespread utility-scale topology to interface solar PV modules to the medium-voltage (MV) grids is the two- or three-level low-voltage (LV) centralized inverter (Figure 4.1) [63-65]. This topology commonly consists of multiple PV arrays (the number of PV modules could easily reach millions of them [66]) attached to a DC-DC converter, increasing the PV array voltage and correctly feeding the low-voltage centralized inverter. Finally, a low-frequency (LF) transformer steps up the LV AC to generate the required voltage for a utility-scale grid (6–36 kV) [67-71].

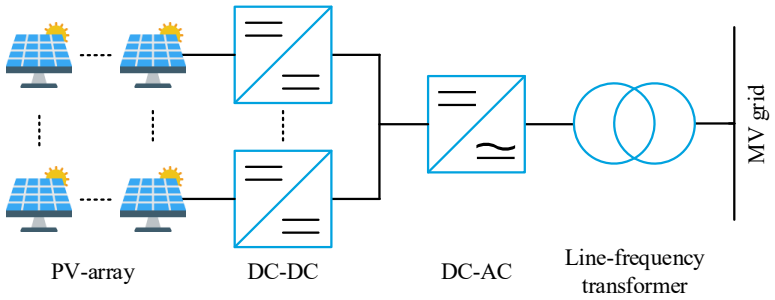


Figure 4.1: Classic two-level inverter for MV grid-tied applications.

This classic configuration faces some disadvantages. The main drawback is the line-frequency transformer. Even though manufacturers are trying to reduce and optimize the transformer's space and volume, it is still huge, making installation and maintenance complex and expensive [68, 72, 73].

Another issue is the limitation (normativity and insulations) to 1 kV on the DC side. In addition, a high total harmonic distortion (THD) makes the use of a line-frequency passive filter mandatory; nevertheless, due to the medium-frequency switching harmonics and high current levels, the filter's efficiency is impaired.

As mentioned, the main problem with the classic configuration is the large transformer; hence, other works have tried to avoid using it [74-77]. These transformerless alternatives use high-rated switches, but even with state-of-the-art

switches (6.5 kV), there is a limit on the inverter's AC output voltage. In the best-case scenario, using a high modulation index, the AC output voltage could reach 3.582 kV; for other modulation indexes, see Table 13. Manufacturers suggest that for an H-bridge inverter design using the 6.5 kV IGBTs, the highest dc-link voltage should be 3.6 kV or lower in consideration of the maximum device commutation voltage for device reliability of 100 failures in time (Vcom@100FIT) [70].

Table 13: Maximum output RMS voltage.

IGBT Rating [V]	DC-link voltage [V]	Output m=0.9 [V]	Output m=0.7 [V]
6500	3600	3240	2520
4500	2250	2025	1575
3300	1800	1620	1260
2500	1200	1080	840
1700	900	810	630
1200	800	720	560
900	600	540	420

Another possibility of implementing the classic configuration to reach MV levels involves the series connection of multiple high-rated switches (Figure 4.2). This approach brings challenges: problematic physical construction, intricate gate driver design, snubber networks, significant filters, and high conduction losses due to the on-state voltage drop [78].

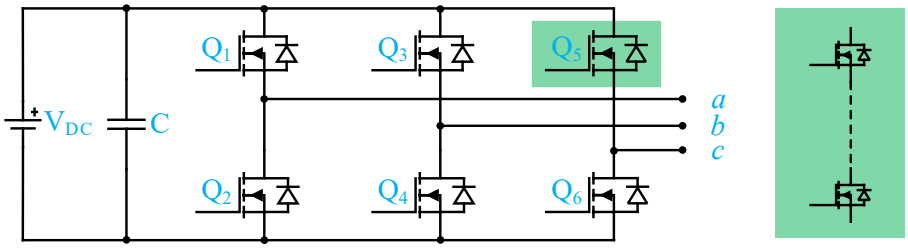


Figure 4.2: 2L-3PH inverter with series connection of MOSFETs.

4.1. BASIC MULTILEVEL INVERTERS

Multilevel converters have been proposed and used to overcome some of the previously discussed problems [72, 79-83]. Multilevel converters show interesting features like direct integration to the MV grid if a fair number of levels are applied; therefore, this converter could be considered a transformerless converter for MV-grid integration [71, 84, 85]. Due to the high number of levels in a staircase form, the

waveform in the converter's output is closer to a sinusoidal signal; this implies that the THD could be minimal [70, 85, 86]. The two formers' features can be achieved without using high-rated voltage switches; in other words, commercial switches can be implemented to achieve the MV levels and a low THD [70]. The only issue to overcome is that the voltage required will increase accordingly to the MV-grid level.

Several multilevel converters have been proposed since the seventies, such as diode clamped, also known as neutral point clamped (NPC), flying capacitor (FC), cascaded H-bridge (CHB), and the modular multilevel converter (MMC), among others. Still, the previous four are fundamental structures [87].

4.1.1. NEUTRAL POINT CLAMPED

Nabae proposed the diode clamped converter [88], and it was the first multilevel topology thoroughly known and popularized, and it remains in use in the industrial environment [89],[90]. This multilevel inverter is widely employed in medium voltage electric drives, railway traction systems, and wind turbines.

The number of voltage levels produced by this converter is m, and requires $m - 1$ capacitors [91]. The capacitors are used as DC sources; therefore, the switches must block the capacitor's voltage. No more than five levels are usually used.

Some features of this topology include that it is fault-tolerant, and the topology presents a low count device compared with MMC and CHB topologies. Some disadvantages of this topology are that the imbalance voltage across the capacitors may increase the total harmonic distortion (THD) of the output voltage and damage the switching devices due to the over voltage breakdown [70]. Some diodes must block more than two times the IGBT's voltage [92]. For unitary power factor and high modulation indexes, the external switches present high switching and high conduction losses while the inner switches mainly present switching losses [93].

4.1.2. FLYING CAPACITOR

The flying capacitor's output levels are generated by the capacitors that float with respect to the ground potential; hence, the switch must block this voltage [94, 95]. This topology provides redundant switching states that can balance the voltage in the flying capacitors [96]. Because of the enormous number of capacitors, the inverter can withstand both short-term outages and severe voltage sags.

This architecture is appealing for some applications, such as high-speed drives and test benches, due to the symmetric distribution of the losses of the switches and the associated high first carrier band of the converter's voltage. The flying capacitor-based inverter features redundancies for inner voltage levels, which means that it can synthesize an output voltage using two or more valid switch combinations. In

addition, the flying capacitor inverter offers phase redundancy, whereas the diode clamped inverter simply has line-line redundancy.

The FC inverters require $(m^2 - 3m + 2) / 2$ auxiliary capacitors; this number is quadratic with the number of the inverter level, making the system impractical, especially for MV and HV applications with more than five output voltage levels. Too many capacitors can reduce the life of the FC converter.

4.1.3. CASCADED H-BRIDGE

This topology was introduced in 1988. The CHB converter is built by cascading k full-bridge (FB) converters and requires multiple isolated DC sources [91]. The number of levels m and DC sources k are related as $m = 2k + 1$; therefore, a high number of DC sources are required [97]. PV farms commonly use multiple PV strings, and each PV string generates its own DC voltage. This converter can produce high-resolution multilevel waveforms with relatively few components. The CHB is as flexible as the MMC converter because the CHB converters can be added or removed. This converter presents redundancy as the previous MLI; there is more than one state that can produce the same voltage level. The previous features make this converter an attractive option for applications like high power drivers, uninterruptible power supplies (UPS), STATCOMs, large-scale PV, and BES systems [98].

The number of levels is not related to the semiconductor's voltage stress because each switch must only block the DC source that supplies power to that full-bridge converter. This converter has a particular need; it requires one isolated DC power supply per FB converter; this could be a disadvantage or an advantage depending on the application [99-102]. The k Isolated DC sources must have the same amplitude; if this is not accomplished, distortion may appear in the converter's output voltages [103]. CHB with different amplitudes are known as asymmetrical CHB inverters, this kind of configuration can generate more output levels with the same number of cascaded HB converters; however, the modularity ability will be lost in this configuration [104, 105].

4.1.4. MODULAR MULTILEVEL CONVERTER

The MMC converter provides an alternative multilevel topology [106, 107]. Three legs integrate an MMC converter, and each leg has two arms, and each arm has k cascaded converters; the MMC has a common DC source. The most common implementation is the HB converter. The main drawback of the use of MMC includes the circulating current between legs. It requires only one DC-source independently of the number of levels. The k sources are supplied by DC-capacitors, where $k = m - 1$.

Switches with low-rate voltage can be used; additionally, high efficiency may be achieved by using low switching frequencies. Moreover, because no clamp

components are required, high numbers of output levels are a key feature of this topology. This converter allows flexibility of design because the voltage can be increased by increasing the number of submodules; in the same sense, there is high reliability because redundancy is inherent in the structure of this power converter [108].

The main disadvantage of the MMC converter is the circulating current between legs. The circulating current can balance the capacitors' voltages depending on the submodule configuration. In order to decrease the converter losses and improve efficiency, the circulating current must be under control. This converter requires a large number of active switches and a large capacity energy storage requirement [109].

4.1.5. IMPLEMENTATION OF CHB

The newest and more complex multilevel converters are based on the previous four, and in some applications, the line-frequency transformer is required to provide isolation, normativity, or security means. The sizing and design methods for eleven cascaded multilevel converters (CMC) were addressed in reference [80]. The authors also provide considerations and a detailed procedure for the power stage. A three-cell seven-level CHB was evaluated in reference [79], and the control method was based on traditional voltage-oriented control. This standard control scheme required the addition of two stages: one stage considers the maximum power point tracking for each module or string, and the other stage controls the DC-link voltages drift. In reference [82], a current-control technique and the switching scheme of a cascaded five-level inverter with a single-phase photovoltaic grid-tied system were introduced. In reference [83], a cascaded H-Bridge multilevel converter for photovoltaic systems without voltage or current sensors at the DC-side was proposed. The effectiveness of the proposed structure was experimentally validated on a 2 kW single-phase seven-level CHB laboratory prototype.

4.2. CHB WITH HF-AC-LINK

In the last decade, HF and MF transformers have been considered to minimize the size and weight of the line frequency transformers in traditional PV farms connected to the grid. However, this HF or MF transformer (also known as AC-link) requires an additional step to transform the MF-AC square voltage to line-frequency AC voltage. There are two options to perform the frequency transformation: the first option is a two-step power conversion (AC-DC/DC-AC), and the second option is a direct-step power transformation (AC-AC).

4.2.1. AC-LINK: TWO-STEP POWER CONVERSION

In this solution, an MF rectifier produces a new DC link that feeds an inverter [110-112]. Reference [72] presents a high-performance solution based on a power electronic transformer (PET); it includes a medium-frequency transformer, DC-links, and multilevel converters. On the low-voltage side, there are different DC-links and each DC-link feeds the cascaded H-bridges. The output of the cascaded H-bridge is connected to the primary of the MF transformer. The MF transformer is designed under a three-phase configuration, but it can be a single-phase design. The transformer's HV side is connected to the MV grid through a multilevel inverter. Some options can be implemented here, for example a CHB converter integrated by a rectifier and an HB converter can be integrated as in Figure 4.3; this solution requires many active switches. An alternative is to implement a unique NPC rectifier that generates a new DC link that can feed a three-phase NPC or FC topology, as shown in Figure 4.4.

In references [68, 81, 85], a three-phase medium-voltage converter (Figure 4.5) with a high-frequency link was proposed for direct grid integration of renewable sources. The magnetic-link guarantees electrical isolation between the PV arrays and the grid.

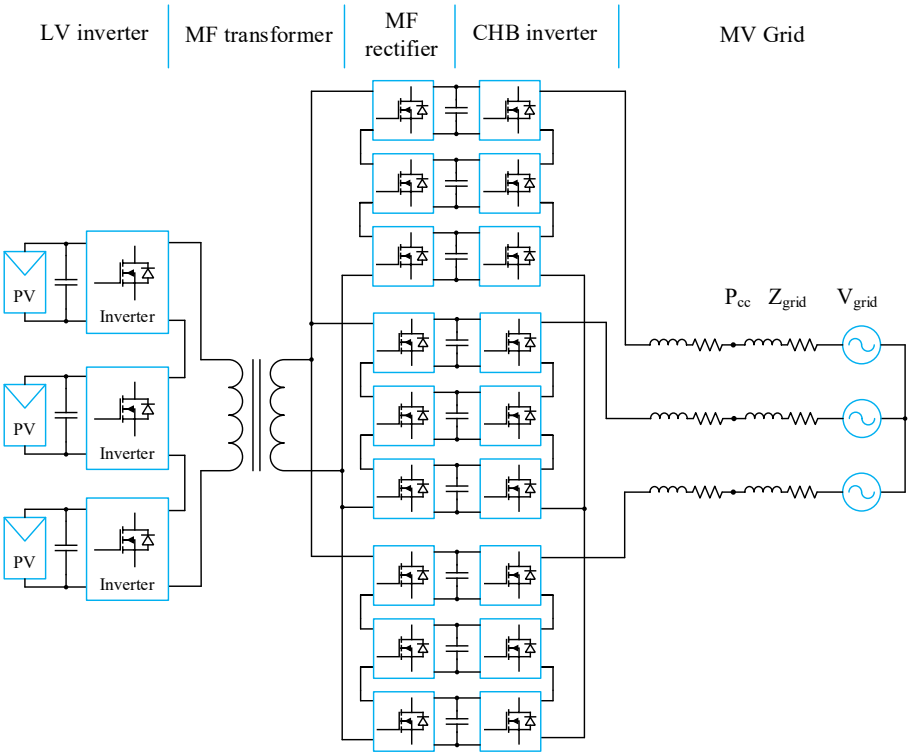


Figure 4.3: PET using MF-AC-link with CHB converters.

The common magnetic link generates several isolated and balanced DC sources for feeding all the H-bridge inverter cells of the MMC converter. The cell is built with a medium frequency rectifier that generates an independent DC-link that feeds an H-bridge converter. There are a couple of options for the primary of the MF transformer; the designer can choose between using only one primary or implementing several primaries. The low voltage module is integrated by PV arrays controlled by a boost converter with a MPPT; later this step-up converter feeds a medium frequency inverter connected to the primary of the MF transformer.

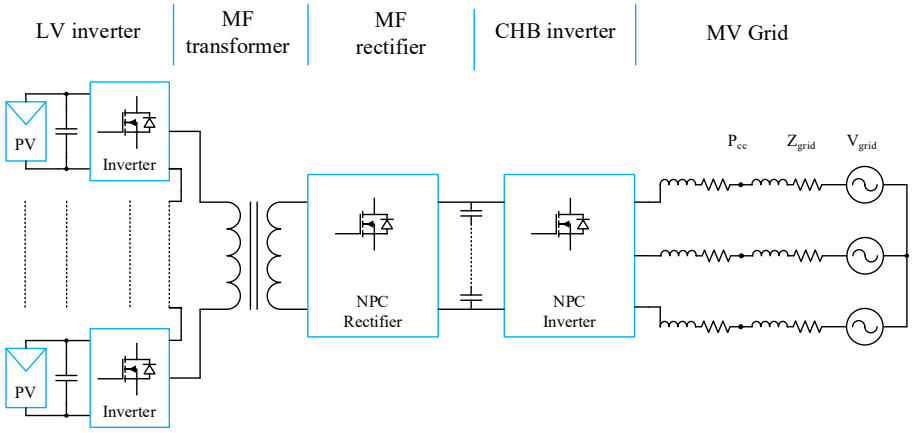


Figure 4.4: PET using MF-AC-link with NPC converter.

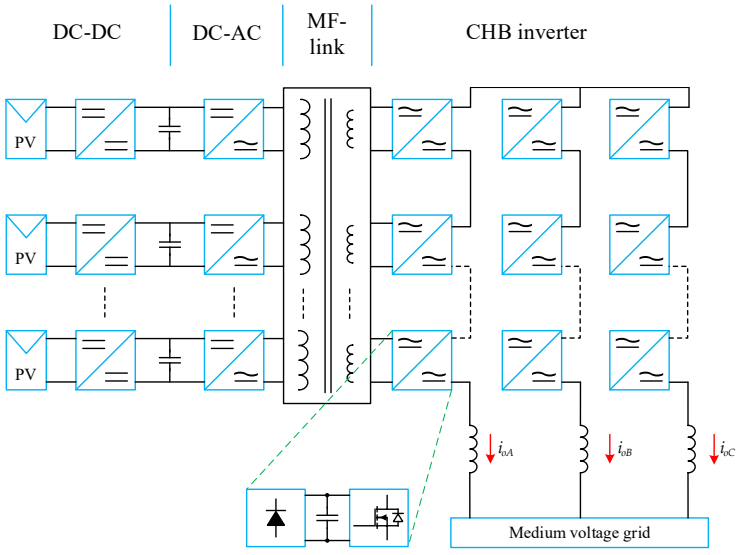


Figure 4.5: MMC inverter with a clear two-step power conversion in the MLI stage.

4.2.2. AC-LINK: ONE-STEP POWER CONVERSION

In reference [97], a direct method conversion was implemented. A direct stage conversion (AC-AC) is the second option to transform an MF-AC voltage into low-frequency AC voltage [92]-[96]. The converter has four stages of energy conversion: DC-DC/DC-AC/AC-AC/AC-AC. The converter uses a switching frequency of 2880 Hz, and the work focuses on designing and operating the converter under unbalanced solar irradiance. The work includes experimental results in three-phase (3PH) and in single-phase (1PH) cascaded configuration, in which it reports an operating of 450 W. Besides, there are tests to validate the area power balancer, but there are no closed-loop experimental tests of the proposed converter neither in three-phase configuration nor cascaded configuration.

4.3. PROPOSED CASCADED DC-AC-AC CONVERTER WITH AC-LINK

Figure 4.6 presents the proposed medium-voltage multilevel power converter with MF-AC links that simplify large-scale PV farms' grid integration.

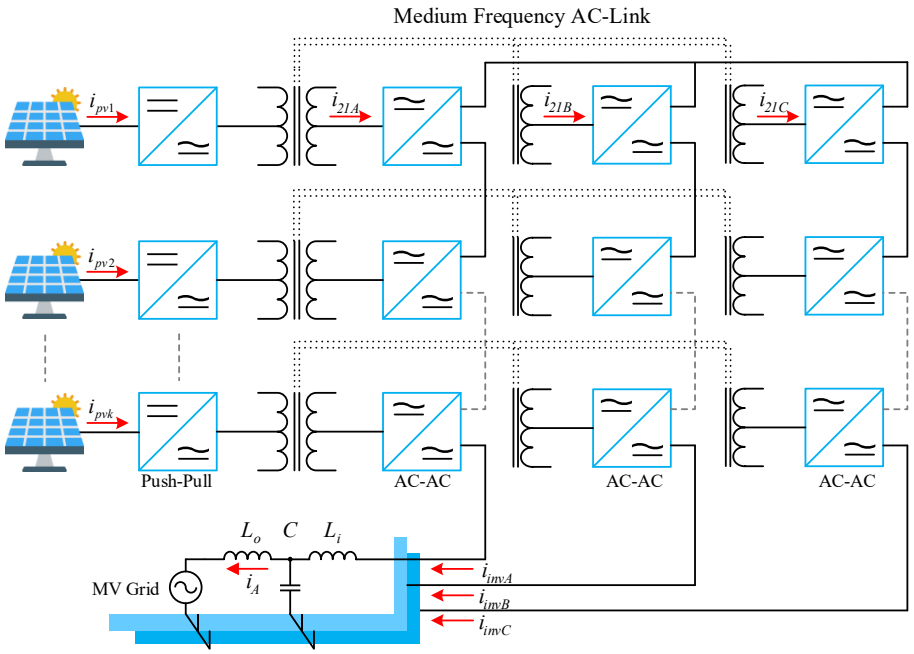


Figure 4.6: Proposed cascaded DC-AC-AC converter with AC-link.

This proposal overcomes some drawbacks related to grid-tie PV plants: use of line-frequency transformers and filters; avoiding using high-rated switches (> 6.5 kW) or the use of series connection switches; elimination of the MF rectifying stage and promoting modularity.

This three-phase multilevel converter is built cascading some converters inter-connected with each other via medium-frequency multiple winding transformers. These transformers generate an MF-AC link. There is only one winding supplied by a square-wave converter on the primary side. There are three windings on the secondary side; each winding plus a suitable converter generates the three-phase output voltages.

This topology has been selected because it has some exciting features:

1) It includes medium-frequency AC links (MF transformers).
2) MF switching allows the size reduction of passive elements.
3) AC-AC direct conversion from MF-AC voltage to LF-AC voltage eliminates a medium-frequency rectifier's necessity.
4) Multiple DC links.
5) Multilevel output voltage that, in consequence, permits interfacing with medium-voltage utilities with a low THD.
6) Does not require a line-frequency transformer.
7) Modularity (multiple DC-AC-AC converters can be cascaded) [113].

4.3.1. GRID TIED MLI WITH AC-LINK

Besides many other state-of-the-art topologies, the one proposed in this work is integrated with some conventional converters that combined present exciting features. In Figure 4.6, the proposal multilevel grid-tied converter with MF-AC links is depicted in the form of a block diagram. The suggested converter facilitates the incorporation of utility-scale PV plants into the MV utility.

This proposed topology is built cascading *k* three-phase DC-AC-AC converters. Some converters integrate this DC-AC-AC structure; one is referred to as the input converter and the others as the output converters. The input and output converters are interconnected through a medium-frequency multiple winding transformer that isolates the PV arrays from the utility. The multiple winding transformer involves four windings. The first winding is the primary, and it is connected with the input converter. The rest of the windings integrate the secondary; thus, the secondary and its corresponding output converter (each winding is connected to one output converter) generate a three-phase electrical system.

To cascade the DC-AC-AC converter and achieve the multilevel output voltage, the converters connected to the MF transformers' secondary windings are cascaded with

their corresponding windings from other multiple winding transformers. The multilevel output voltage will present a low THD that depends on how many converters are cascaded [114, 115]. This work considers three cascaded converters to simplify the analysis and the simulations' running time, but in general, the number of cascaded converters (cells) may be *k*.

4.3.1.1 Single-Phase DC-AC-AC Converter Cell

Figure 4.7 shows the block diagram of the DC-AC-AC converter in a single-phase configuration to understand how the proposed topology works. The series connection of more than one 3PH DC-AC-AC converter builds the multilevel structure.

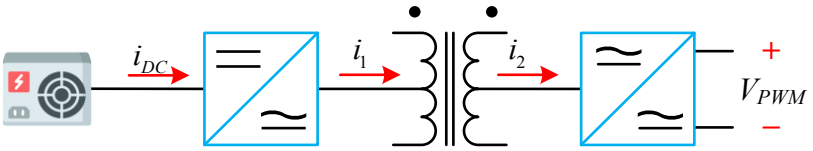


Figure 4.7: Block diagram of a singles-phase DC-AC-AC converter cell.

The block diagram is explained from left to right because of the power flow from the PV plant flows in that direction:

- The PV modules are the first stage; they are interconnected in series-parallel arrays to satisfy the design and regulations' power levels. Ideal DC power supplies replace the PV modules for this explanation.
- The second stage converts the DC voltage to a medium-frequency square AC voltage. Many converters can do this work: half-bridge, full-bridge, push-pull, flyback, dual-active-bridge, and others. Push-pull converter is selected for this stage due to low-count of power switches.
- The third stage consists of a ferrite-based medium-frequency transformer, isolating and stepping up the voltage. The primary winding is plugged into stage two, and the secondary winding feeds stage four.
- The fourth stage has the task of converting an MF-AC voltage to a low-frequency AC voltage. As mentioned in section 4.2, there are two methods to accomplish that task: a two-step (involves an MF rectifier and an inverter) and a direct AC-AC approach. The direct method could eliminate the MF-rectifier, get bidirectional power flow, and improve efficiency.

Figure 4.8 presents a schematic view of the DC-AC-AC converter. As in Figure 4.7, the PV arrays were interchanged by ideal DC power supplies to facilitate the explanation. The DC power supply feeds a push-pull converter that works as an MF square wave voltage generator (second stage). The push-pull converter uses a transformer action to transfer power from the primary side to the secondary side. This

converter requires two switches operating alternatively (Q_1 and Q_2); this means that only one switch is turned ON for the entire duration of the switching period.

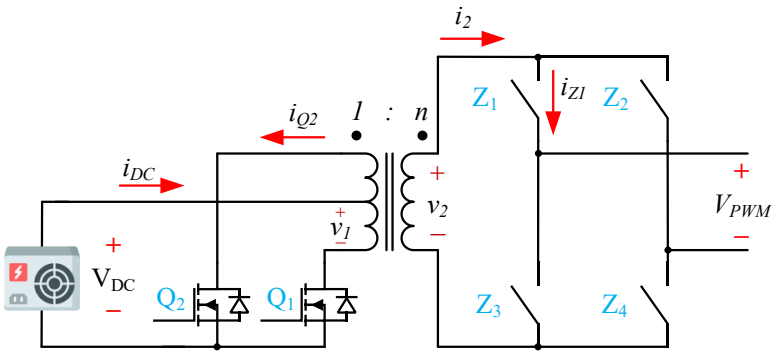


Figure 4.8: A single-phase DC-AC-AC converter's cell schematic.

This operation could be reflected in lower conduction losses. In addition, the symmetric configuration of the switches reduces the radiated electromagnetic emissions (also, minimizing the transformer's leakage inductance is vital to minimize the electromagnetic interference). Moreover, the implementation of the two identical low-side switches requires only one DC supplier for the gate driver. The transformer action regulates the output voltage in v_2 in a feed-forward manner; therefore, the output voltage solely depends on the transformer turn ratio and the DC power supply value. The magnetic core is efficient because the flux accumulation in one polarity is canceled in the other due to the bipolar operation. One overcome is that the switches have to support two times the voltage of the DC power supply. Due to the features mentioned above, the push-pull converter is implemented in the second stage.

Regarding the fourth stage, a couple of converters can directly convert a MF-AC voltage to line-frequency voltage (also known as AC-AC converters or Matrix converters); the half-bridge converter, and the full-bridge are the most widespread. Because of the push-pull converter, it is impossible to ensure zero volts systematically; only +VDC and −VDC are possible; therefore, it is necessary to choose the full-bridge converter. The final objective of this converter is to inject the sinusoidal current waveform into the utility.

4.3.1.2 Modulation Strategy for a Single-Phase DC-AC-AC Converter

It is essential to determine that the standard sign over the load voltage is always retained. Hence, to operate the converter correctly, the commutation strategy should change the polarity on v_2 from the load point of view. For example, consider Figure 4.9, where the active devices are in blue color; if the voltage on V_{PWM} is required to

be positive when v_2 is negative, then Q_2, Z_2, and Z_3 must be turned ON; in this case, the voltage on the V_{PWM} terminals will be negative.

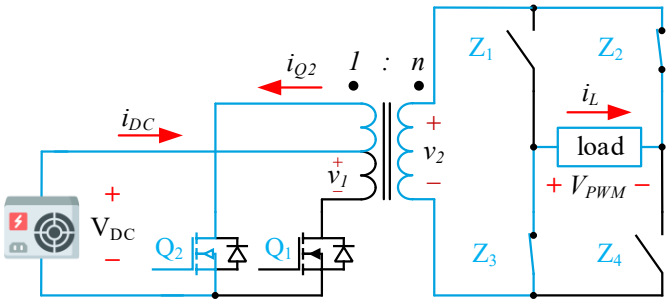


Figure 4.9: Operation of the DC-AC-AC converter.

The modulation implemented on the AC-AC converter is a variant of the unipolar sinusoidal PWM (SPWM). Compared with bipolar SPWM, the unipolar SPWM can effectively double the switching frequency. This benefit is appreciated in the harmonic spectrum of the output voltage waveform. The harmonic components related to the switching frequency and their sidebands are canceled; besides, the dominant harmonic located at the double the switching frequency is withdrawn but not their bands [55].

The modulation strategy must synthesize a square MF-AC voltage from v_2 into an equivalent unipolar sinusoidal pulse width modulation (SPWM) in the V_{PWM}'s terminals of the full-bridge converter. The input and output converters must be synchronized and commute at the same frequency rate to reach this objective.

There are two switching strategies to operate an AC-AC converter: switching controlled by current and switching controlled by voltage [116-118]. The second one is the most convenient solution for the proposed DC-AC-AC converter because the push-pull converter and the full-bridge converter can be synchronized easily [119].

Hence, with the selected strategy, the synchronization signal v_2, and the two control SPWM signals (S_1 and S_2) is possible to generate an adequate switching pattern for the matrix converter. In reference [120], the complete commutation strategy is addressed.

Due to the fact that the actual DC-AC-AC converter is a three-phase system, there are three AC-AC converters. The previous strategy is extended using three modulation waveforms and its counter-phase waveforms; thus, each pair of the modulated signal is shifted 120° from each other.

The output voltage of the proposed converter Figure 4.6 is multilevel; hence, it is essential to apply a proper modulation technique. Due to its benefits [121], phase-

shifted multicarrier sinusoidal PWM (PSPWM) modulation is chosen. An attractive feature is the effective switching frequency $(m-1)f_c$ obtained with the PSPWM modulation in the output voltage V_{PWM}.

4.3.2. SIZING OF THE THREE-PHASE DC-AC-AC CASCADED CONVERTER

As stated earlier, multilevel topologies allow for high-voltage levels, effectively increasing the output frequency [55, 122, 123], and low THD due to the lower harmonic content. Other exciting features come from three-phase systems; the magnetic link makes it possible to cancel the single-phase component found twice in the line frequency in the DC waveform. As stated previously, only three cascaded converters are taken into consideration to simplify the design and specifically the simulation complexity.

In Table 14 are the main parameters that this design will consider for a seven-levels 3PH DC-AC-AC converter.

Table 14: Design parameters for the 3PH AC-AC-AC cascaded converter.

Parameter	Acronym	Value
Rated Power	P_o	324.16 kW
Output voltage	V_{LL}	13.20 kV
DC-link voltage	V_{DC}	1.00 kV
Switching frequency	f_{sw}	9.96 kHz
Output levels	m	7
Output frequency	f	60 Hz

Let m be the number of voltage levels at the output, then the required number of independent DC sources is:

$$k = \frac{(m-1)}{2}, \tag{4.1}$$

and each independent DC source should have the same voltage amplitude. Due to each AC-AC converter producing a fundamental frequency component V_{o1}, V_{o2}, and V_{o3}, then the V_o is given by the output voltages addition of each cascaded converter:

$$V_o = V_{o1} + V_{o2} + V_{o3}. \tag{4.2}$$

Considering that the phase to neutral voltage (V_o) is $V_o = V_{op}\ sin(\omega_o t)$, with $\omega_o = 2\pi f$. It is known from the three-phase electrical system that the rated output power of a converter is:

$$P_o = \frac{3V_{op}I_{op}}{2} = \sqrt{3}V_{LL}I_o = 3V_oI_o, \tag{4.3}$$

and when contemplating the values from Table 14, the root mean square (RMS) output current (I_o) results in 14.17 A, and the RMS V_o is 7.62 kV. With the output current, the equivalent resistive load per phase is:

$$R_o = \frac{3V_o^2}{P_o} = 537.52\,\Omega. \tag{4.4}$$

When the modulation index is 0.9, the transformer turns ratio results in:

$$n = \frac{V_{op}}{km_aV_{DC}} = 3.99, \tag{4.5}$$

and it should warrant the system's operation with a minimum voltage in the input supply and the maximum load, considering that the modulation index at 0.9 is high. Hence, let n be 4.5; this results in a new modulation index of 0.80.

As the value of the DC source is known as well as the transformer turn ratio; then, the MF-transformer's voltages across the three secondary windings are:

$$|v_2| = nV_{DC} = 4.50\,kV, \tag{4.6}$$

and its corresponding peak current can be calculated as

$$i_{2p} = \sqrt{2}I_o = 20.05\,A. \tag{4.7}$$

If there are no losses in the process of energy transformation, the average and peak current [124] in each of the k DC input supplies are:

$$I_{DC} = \frac{P_o}{kV_{DC}} = 72.03\,A \tag{4.8}$$

$$I_{DCp} = \frac{3ni_{2p}}{\sqrt{2}} = 191.40\,A \tag{4.9}$$

correspondingly. The selection of the DC-link capacitor is calculated as follows:

$$C_{link} = \frac{P}{2\pi f \Delta V_{DC} V_{DC}} = 6879\,\mu F. \tag{4.10}$$

Finally, in order to reduce the THD produced by the high switching frequency and have a pure sinusoidal waveform at the output, a second-order LC filter is placed between the power converter and the resistive load. Because PSPWM technique is implemented, and the output voltage is seven-level, the first carrier group produced by V_{PWM} is expected at:

$$f_{1st} = f_{sw}\left(m-1\right) = 60\,\text{kHz} \tag{4.11}$$

Choosing the cutoff frequency (f_{cutoff}) one decade before the switching frequency is a common practice. Then, let f_{cutoff} be 6 kHz. The LC filter configuration gets an attenuation of -40 dB/decade with previous parameters. The attenuation effect of the LC filter can be increased by decreasing the filter cutoff frequency against the switching frequency according to

$$-40\log\left(\frac{f_{1st}}{f_{cutoff}}\right)\text{db}. \tag{4.12}$$

Once the cutoff frequency is selected, the next step is calculating the passive elements of the filter. The equations are derived from the transfer function of a second-order filter considering a resistive load. The derivation of the equations is described in [125]. The capacitance and the inductance are calculated below:

$$L_o = \frac{\sqrt{2}R_o}{2\pi f_{cutoff}} = 20.16\,\text{mH}, \tag{4.13}$$

$$C_o = \frac{1}{\left(2\pi f_{cutoff}\right)^2 L_o} = 34.9\,\text{nF}. \tag{4.14}$$

4.3.3. CONTROL DESIGN OF THE THREE-PHASE DC-AC-AC CONVERTER

This section aims to design the current and voltage controller for the 3PH DC-AC-AC converter in standalone mode. As demonstrated during this chapter, the DC-AC-AC converters behave essentially the same as a voltage source inverter; hence, for control proposes, the DC-AC-AC converter will be treated as a black box with a gain directly related to the MF transformer's turn ratio.

4.3.3.1 Modeling

The three-phase system of Figure 4.10 can be modeled as two independent single-phase systems based on the *abc* to *αβ* transformation [126]. The control structure is simplified and presented in Figure 4.11, and it consists of an inverter model plus the LC filter and the voltage and current controllers. The model is the averaged differential equations over one switching cycle of the valid if the model is considered ideal.

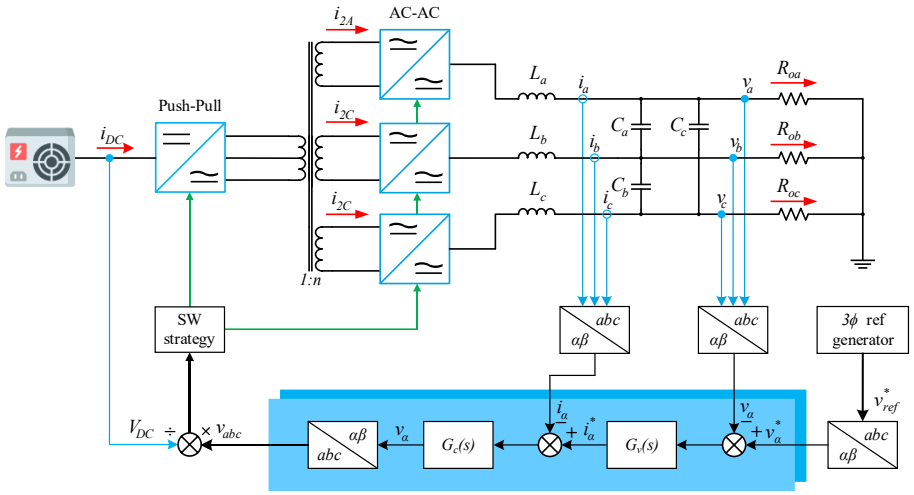


Figure 4.10: Block diagram of the voltage-current controllers of the three-phase DC-AC-AC converter.

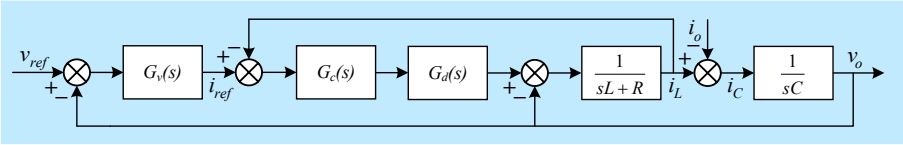


Figure 4.11: Closed-loop representation of the voltage and current PR compensators and the LC filter of the 3PH DC-AC-AC converter.

Employing Manson's theorem, the block diagram of the previous figure can be reduced, and the closed-loop voltage dynamic transfer functions are obtained. To get the transfer function, the next set of equations are defined:

$$\left(V_{ref} - V_o\right) G_v(s) = I_{ref} \tag{4.15}$$

$$\left(I_{ref} - I_L\right) G_i(s) G_d(s) = V_{abc} \tag{4.16}$$

$$\left(V_{abc} - V_o\right)\frac{1}{sL+R} = I_L \tag{4.17}$$

$$\frac{I_L - I_o}{sC} = V_o \tag{4.18}$$

Where V_{ref} is the voltage reference, I_o is the output current, and V_o is the output voltage (capacitor voltage). $G_v(s)$, $G_i(s)$ are the voltage and the current controllers, respectively. $G_d(s)$ delay in the system, and it is integrated by two quantities, the first one represents the sampling, computation, and updating of registers and the zero-order hold (ZOH) delay, which is considered as one sampling period T_s while the second quantity is the modulator block which adds an additional 0.5 T_s delay. Then, the total delay in the control loops is 1.5 T_s [127], and its transfer function is given below.

$$G_d\left(s\right) = \frac{1}{1+1.5T_s s} \tag{4.19}$$

By using the superposition theorem from the equation (4.18), let the current source (i_o) be *0*; then,

$$I_L = sV_oC \tag{4.20}$$

With the previous result, the equation (4.17) is transformed to

$$V_{abc} = V_o\left(s^2LC + sRC + 1\right) \tag{4.21}$$

Using equations (4.20) and (4.21) in the equation (4.16) results

$$I_{ref} = \frac{V_o\left(s^2LC + sC\left(R + G_i\left(s\right)G_d\left(s\right)\right) + 1\right)}{G_i\left(s\right)G_d\left(s\right)} \tag{4.22}$$

Finally, substituting the previous result in the equation (4.15), and after some algebraic operations

$$V_o = \frac{G_i\left(s\right)G_v\left(s\right)G_d\left(s\right)}{s^2LC + sRC + G_i\left(s\right)G_d\left(s\right)\left(sC + G_v\left(s\right)\right) + 1}V_{ref} \tag{4.23}$$

The same procedure is followed but now, considering that the voltage source (V_{ref}) is equal to zero, which leads to

$$V_o = -\frac{sL + R + G_i(s)G_d(s)}{s^2LC + sRC + G_i(s)G_d(s)\left(sC + G_v(s)\right) + 1} I_o \tag{4.24}$$

By combining equations (4.23) and (4.24)

$$\begin{aligned} V_o = {} & \frac{G_i(s)G_v(s)G_d(s)}{s^2LC + sRC + G_i(s)G_d(s)\left(sC + G_v(s)\right) + 1} V_{ref} \\ & - \frac{sL + R + G_i(s)G_d(s)}{s^2LC + sRC + G_i(s)G_d(s)\left(sC + G_v(s)\right) + 1} I_o \end{aligned} \tag{4.25}$$

4.3.3.2 Control technique

Some controllers are overloaded by intricate computational requirements or are somewhat parametric sensitivity or both; on the contrary, simple proportional-integral (PI) controllers are susceptible to be problematic involving steady-state error in the stationary frame and the need to decouple dependency; moreover, they are unable to significantly reduce the low order harmonics component due to bandwidth limitations. PI controllers have been improving by adding feed-forwards paths or by increasing the gains these methods can increase the bandwidth, but the consequences are the stability limits [126, 128]. Moreover, the injected current to the grid can get distorted because the feedforward path if the grid voltage is distorted [129]. The synchronous frame is another solution to the above-mentioned drawbacks; it operates on DC quantities and provides infinite gain which is translated to zero steady-state error. The disadvantage of this frame is that it requires several frame transformations which could lead to overwhelming some microcontrollers.

A proportional resonant (PR) controller is a proportional gain plus a resonant part tuned at a desired frequency where it introduces an infinite gain. The implementation of PR controllers allows for a good performance in tracking the converter's sinusoidal reference in the stationary frame with practically the same frequency response as the synchronous frame; additionally, it can be implemented on low-cost microcontrollers.

Then the objective of a PR controller is to reach zero phase and magnitude error, and this can be done by transforming a DC compensator (PI controller) into an AC compensator. The transformation method was developed by Daniel Zmood et al. in [130]. The resulting transformation is the transfer function of the PR controller:

$$G_{PR\_ideal} = K_p + \frac{2K_i s}{s^2 + \omega_o^2} \tag{4.26}$$

If the ideality of the integrator of a PI controller is not possible, then the integrator can be approximated to a low pass transfer function, resulting in the following transfer functions for the PI and the PR controllers respectively

$$G_{PI}(s) = K_P + \frac{K_I \omega_c}{s + \omega_c} \tag{4.27}$$

$$G_{PR}(s) = K_P + \frac{2K_I \omega_c s}{s^2 + 2\omega_c s + \omega_o^2} \tag{4.28}$$

A modified version of (4.28) was presented in [131], and it is the PR transfer function that is used in this work for the voltage controllers $G_v(s)$ of (4.15)-(4.25), Figure 4.10 and Figure 4.11. The transfer function is displayed below:

$$G_v(s) = k_p + \frac{K_I s}{s^2 + 2\omega_c s + \omega_o^2} \tag{4.29}$$

The control diagram of Figure 4.11 works as follows. The current controller's inputs are the compensated difference between the measured and the references of the voltage controller. The voltage controller's input is the output of the voltage compensator (the difference between the measured voltage and the three-phase voltage generator). In this case, the filter's capacitor voltage and the filter's inductor current are the feedback signals that the controller requires.

The inverter reference voltages in $\alpha\beta$ form are the outputs from the current controller, which are transformed back to stationary three-phase coordinates and divided by the DC power supply voltage to generate a modulated signal between 0 and 1. Finally, the modulated signals are sent to the SPWM generator, where each modulated signal is compared with a carrier waveform at a given switching frequency and generates the PWMs. Before the PWM reaches the gate drivers, the signals are processed through a switching strategy, as explained in section 4.3.1.2.

Fifth, seventh, and eleven-order harmonic compensators could be added to (4.29) in order to improve the power quality of the output voltage waveform under nonlinear loads. This is done by cascading h resonant blocks tuned at the desired harmonic frequency (for example 5, 7, 11); therefore, the new transfer function would be

$$G_{PR\_h}(s) = k_p + \sum_{h=5,7,11} \frac{K_{Ih} s}{s^2 + 2\omega_c s + (h\omega_o)^2}, \tag{4.30}$$

where h is the harmonic to be compensated and K_{Ih} is the individual resonant gain. Harmonic compensators do not affect the dynamic of the (4.29), because the cascaded

resonant block only compensates for the selected frequency and close surroundings. The procedure for tuning the resonant gains of (4.31) is the same that the one will be explained in section 4.3.3.5. In general, the gain of the individual harmonic compensators must be selected relatively high (as high as the fundamental frequency's gain) [126, 132, 133].

4.3.3.3 Methodology for controller design

The following considerations are taken into account to design the controller under frequency analysis.

- With the bode plot of the open-loop transfer function, the designer should try to obtain the maximum open-loop gain at any frequency. As a result, the effect of the perturbation on the control system will be minimized. Moreover, the cross-frequency should be as high as possible; but one decade lower than the switching frequency; thus, the system responds fast.
- The bode plot of the close loop transfer function reflects if the controller can track the reference, are the desired frequency. At the desired frequency (f_c) the magnitude should reach 0 dB. At lower frequencies of f_c it can be said that the system can reject DC components. If the gain is high enough, then the system can as well reject HF components.

As explained in the previous section, the implemented controllers are resonant proportional controllers. The resonant term in (4.26) - (4.29) provides minimal gain outside their band pass region due to the narrow band frequency response. Therefore, a proportional gain term is required. The larger the proportional gain, the faster will be the transient response.

The general methodology for designing the controllers is the following

1. Using the open-loop transfer function, the proportional gain will be chosen such that the controller is stable and provides a good transient response.
    a. The damping response increases as the phase margin
    b. Transient response is equivalent to the desired phase margin. A rule of thumb is to select a phase margin between 30 and 60 degrees.
2. Design the resonant component that gives the desired steady-state, phase, and amplitude error without making the phase margin too small
3. Using the closed loop transfer function, verify the cross-frequency where the amplitude crosses the 0 dB line. The cross-frequency should be one decade behind the switching frequency

The inner closed-loop bandwidth is related to the outer loops and should be five to ten times larger. Otherwise, undesired effects such as nonminimum-phase behavior or intensive ringing may be obtained [53].

The open-loop transfer function is obtained from Figure 4.11, but without taking into account the feedback loop from V_o to V_{ref}, the resulting block diagram is found in the figure below:

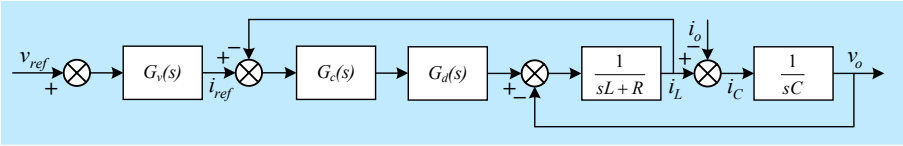


Figure 4.12: Block diagram for obtaining the system loop gain.

In order to obtain the system loop gain transfer function, the procedure explained to obtain the equation (4.25) is followed. The basic equations for obtaining the transfer function are the next:

$$\left(V_{ref}G_v(s)-I_L\right)G_c(s)G_d(s)=V_{inv} \tag{4.32}$$

$$\left(V_{inv}-V_o\right)\frac{1}{sL+R}=I_L \tag{4.33}$$

$$\left(I_L-I_o\right)\frac{1}{sC}=V_o \tag{4.34}$$

After some algebraic operations, the transfer function of the system loop gain is obtained:

$$T(s)=\frac{V_o}{V_{ref}}=\frac{G_v(s)G_c(s)G_d(s)}{s^2LC+sC\left(R+G_c(s)G_d(s)\right)+1} \tag{4.35}$$

4.3.3.4 Current control loop

The controllers are designed with the parameters listed in Table 15:

Table 15: Parameters used for the controller design.

Parameter	Acronym	Value
Inductance	L	8.6 mH
Inductance parasitic resistance	R	0.1 Ω
Capacitance	C	9.0 μF
DC-link voltage	V_{DC}	650 V

Switching frequency	f_{sw}	10 kHz
Output frequency	f	50 Hz
Rated Power	P_o	10 kW
Output voltage	V_{LL}	400 V

From Figure 4.11, consider the loop gain for the current loop (refers to Figure 4.13). For this design, $G_c(s)$ is a pure proportional controller k_{pi}. Then, the transfer function of such loop is given by:

$$G_{i\_ol}(s) = \frac{I_L}{I_{ref}} = G_c(s) G_d(s) \frac{1}{sL + R} \tag{4.36}$$

Where $G_d(s)$ was defined in the equation (4.19), a gain sweep is performed for tuning the parameter k_{pI}, and the bode plots of $G_{i\_ol}(s)$ are arranged in Figure 4.14. The sweep gain resulted in the selection of $k_{pI} = 54$, which shows a reasonable phase margin of 53.2 deg.

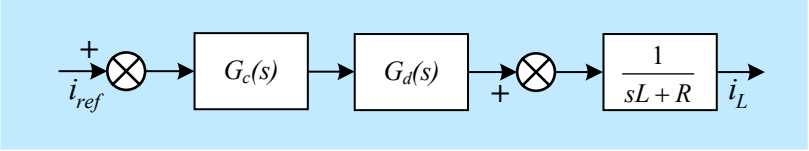


Figure 4.13: Block diagram loop gain of the internal loop.

In order to verify the crossover frequency of the inner loop, the closed-loop transfer function of $G_{i\_ol}(s)$ is required:

$$G_{i\_cl}(s) = \frac{\frac{I_L}{I_{ref}}}{1 + \frac{I_L}{I_{ref}}} = \frac{G_c(s) G_d(s) \frac{1}{sL + R}}{1 + G_c(s) G_d(s) \frac{1}{sL + R}} \tag{4.37}$$

The bode plot of $G_{i\_cl}(s)$ is depicted in Figure 4.15 and shows that the crossover frequency is 995 Hz, which is practically one decade below the switching frequency; therefore, k_{pI} has been tuned accordingly to the desired objective.

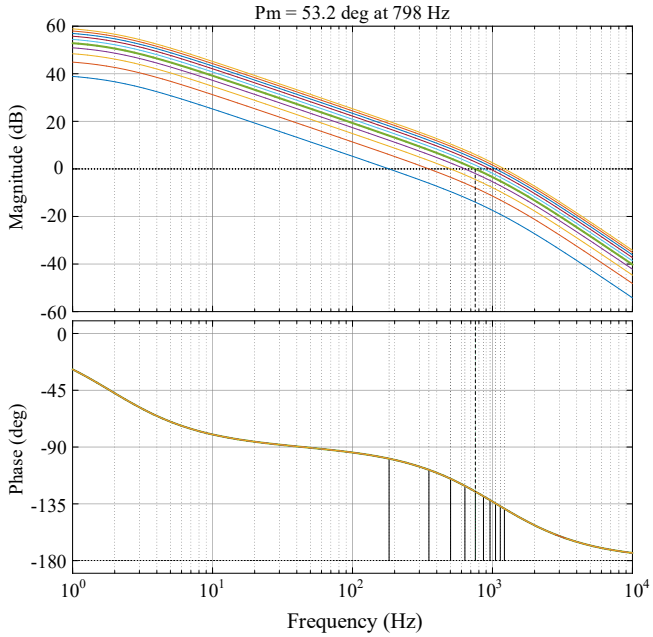


Figure 4.14: Bode plots: sweep gain of the internal loop gain transfer function $G_{i\_ol}(s)$.

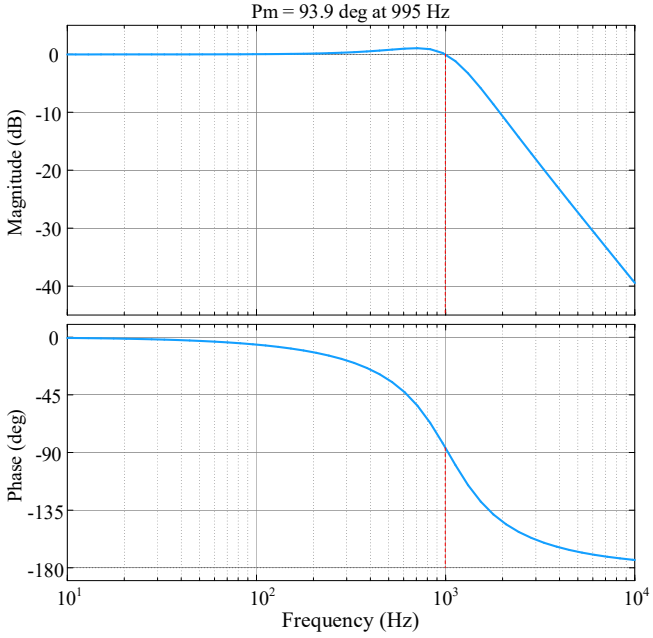


Figure 4.15: Bode plot of the closed-loop inner loop transfer function.

4.3.3.5 Voltage control loop

In order to design the voltage control loop, it is necessary to obtain the loop gain transfer function of such loop; hence, consider the block diagram of Figure 4.16, where the closed current loop is already taken into account and defined by $G_{i\_cl}(s)$. The transfer function of such a loop is given by:

$$G_{v\_ol}(s) = G_v(s) G_{i\_cl}(s) \frac{1}{sC} \tag{4.38}$$

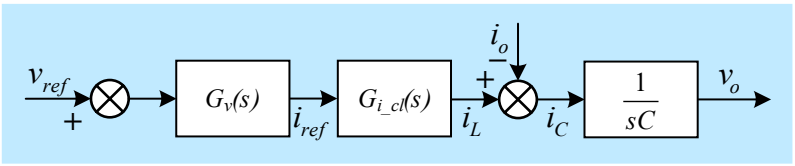


Figure 4.16: Block diagram loop gain of the external loop.

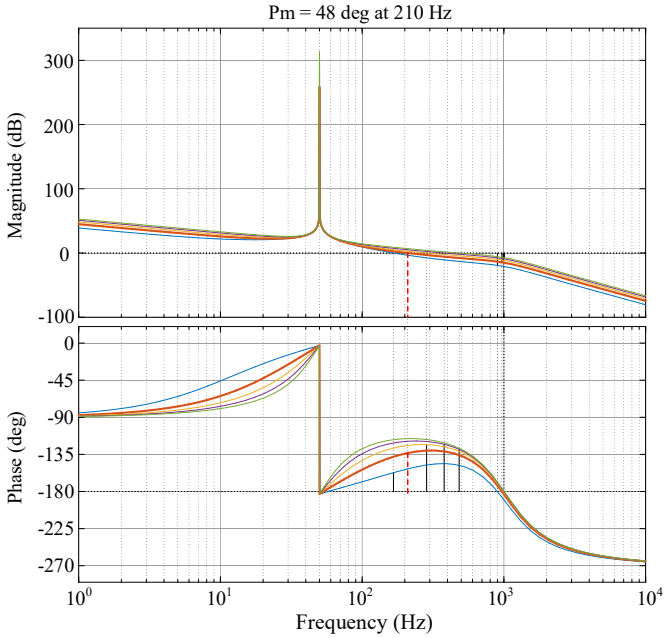


Figure 4.17: Bode plots: k_{pV}'s sweep gain of the external loop gain transfer function $G_{v\_ol}(s)$.

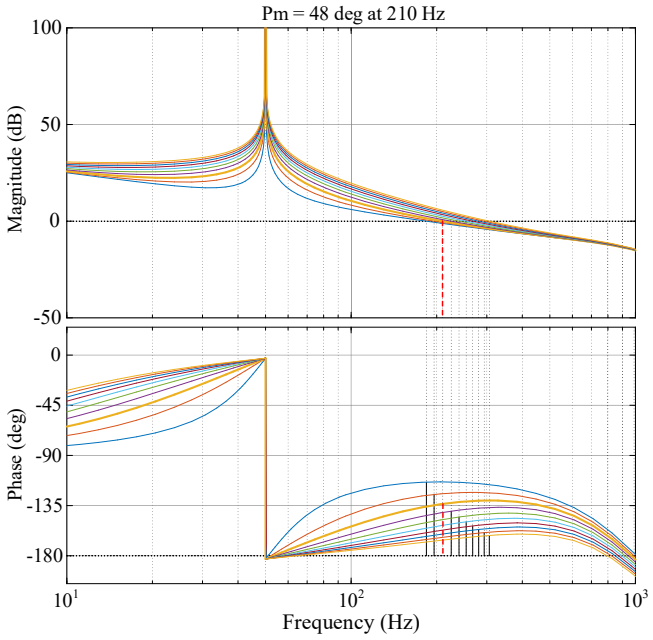


Figure 4.18: Bode plots: k_{pI}'s sweep gain of the external loop gain transfer function $G_{v\_ol}(s)$.

For tuning the parameter k_{pV}, a gain sweep is performed considering $k_{iV} = 7.45$, then the bode plots of $G_{v\_ol}(s)$ are arranged in Figure 4.17. The sweep gain resulted in the selection of $k_{pV} = 0.01$, which shows a reasonable phase margin of 48 deg.

Once the proportional gain is selected, it is time to design the resonant term. The Bode plot of the system loop gain for different values of k_{iV} is depicted in Figure 4.18. As shown, all of the values of k_{iV} provide a high enough loop gain at the fundamental frequency, which guarantees accurate reference tracking while keeping the phase margin at 48 deg. Therefore, $k_{iV} = 7.45$ is selected.

In order to verify the crossover frequency of the external loop, the closed-loop transfer function of $G_{v\_ol}(s)$ is required:

$$G_{v\_cl}(s) = \frac{G_{v\_ol}(s)}{1 + G_{v\_ol}(s)} = \frac{G_v(s) G_{i\_cl}(s) \frac{1}{sC}}{1 + G_v(s) G_{i\_cl}(s) \frac{1}{sC}} \tag{4.39}$$

The bode plot (Figure 4.19) of $G_{v\_cl}(s)$ shows that the crossover frequency is 262 Hz, which is below the crossover frequency of the inner loop; therefore, k_{iV} is tuned accordingly to the desired objective.

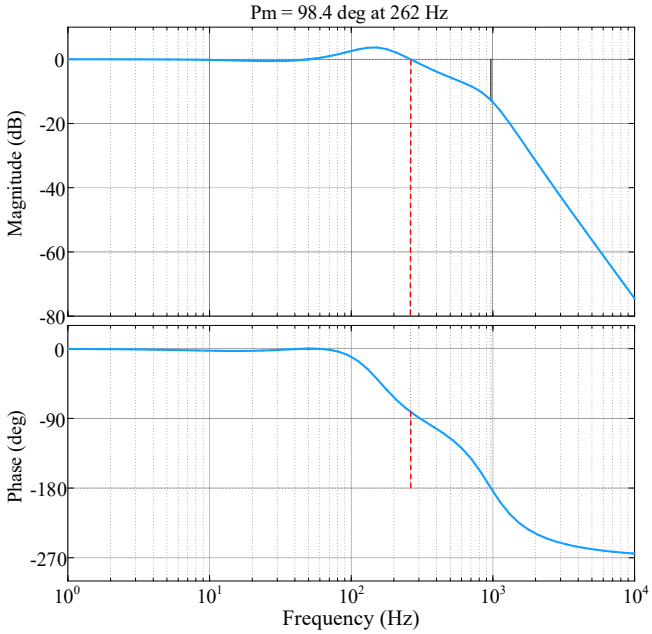


Figure 4.19: Bode plot of the closed loop transfer function (4.38).

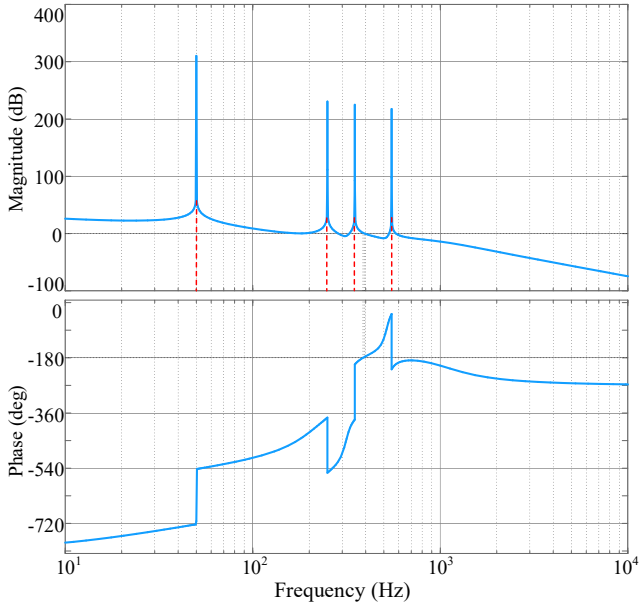


Figure 4.20: Bode plot of the open loop transfer function with HC.

If harmonic compensation is taken into account, the bode plot of (4.38) considering $G_v(s) = G_{PR\_h}(s)$ with $k_{pV} = 0.01$ and $k_{iV} = 7.45$ is depicted on Figure 4.20.

4.3.4. CONTROL STRATEGY OF THE THREE-PHASE SEVEN-LEVEL DC-AC-AC CONVERTER WITH AC-LINK

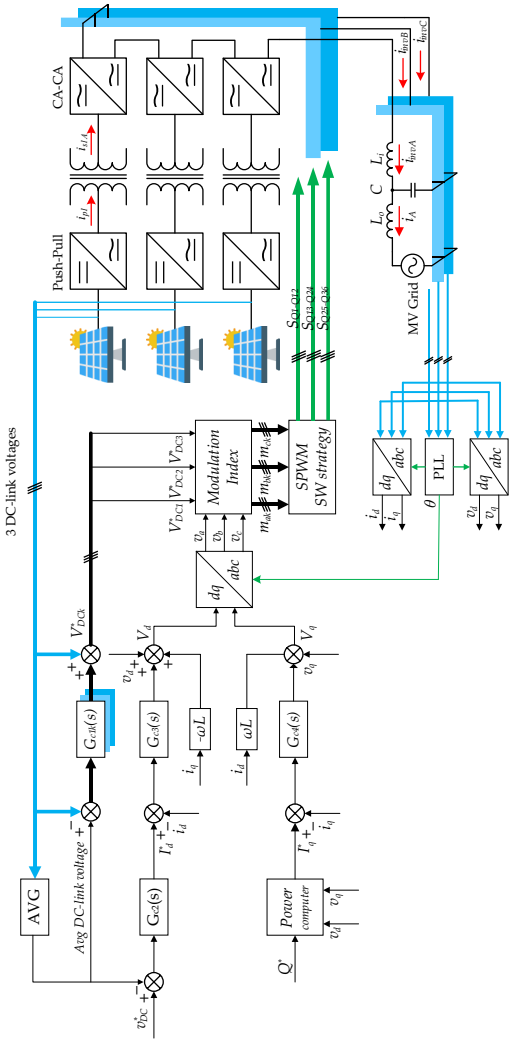


Figure 4.21: Control scheme of the proposed 3PH DC-AC-AC cascaded converter.

Figure 4.21 displays the control scheme of the proposed converter. A 3PH phase-locked loop (PLL) is implemented to synchronize the converter with the grid; an inductance-capacitance-inductance (LCL) filter interconnects the multilevel converter

with the utility. As usual in grid-tied converters, one external loop and one internal regulates the converter by means of the Voltage Oriented Control (VOC) under the synchronous rotating reference frame.

The cascaded DC-AC-AC converters will work together as a controlled current source feeding the utility, as shown in Figure 4.6. Because PV arrays work as a current source, their voltages are dependable on the current extracted and the level of light intensity; in other words, the PV arrays' output voltages depend on the operating point in the PV curves (current versus voltage and power versus voltage). Note that the cascaded DC-AC-AC converters have the same circulating current in each phase (i_a, i_b, and i_c); therefore, it is challenging to carry an independent grid current control loop to regulate each DC-link voltage. Thus, the k DC-link voltages' average must be computed into a single cascaded grid current control loop as was proposed in [134].

In practice, the current control loop (the inner loop) should be designed to be faster than the outer loop to follow the given reference. Hence, the inner loop controls the current injected to the utility employing a simple PI controller through $dq \rightarrow abc$ transformation, this considering decoupling between I_d and I_q control. v_a, v_b, and v_c are generated after the transformation from dq frame to abc of the control signals V_d and V_q.

In the external control loop $G_{c2}(s)$, the k DC-link voltages' average is regulated to control the cascaded converters' output power. If the DC-link is controlled to be constant, then the energy extracted from the PVs can be injected into the grid by charging and discharging the DC-link capacitors. To achieve this, the PV power and the active output power should be in equilibrium employing the instantaneous power theory [135]. The outer control loop will generate the current reference for the inner loop $G_{c3}(s)$. The previous sentence means that the deviation of the average of the k DC-link voltages from the reference value is reflected in the inner current loop to adjust the control signals V^*_d and V^*_q.

The signals v_a, v_b and v_c cannot be directly applied to the SPWM generator to control the converter; if this happened, the DC-link capacitors would suffer a voltage deviation because of the different operating conditions created by unequal power distribution between the cells. Commonly there are two types of power imbalance: per cell and per phase.

Because of this converter's nature and configuration, the per-phase power imbalance does not occur; this is an outstanding advantage compared to other topologies in state-of-the-art. In those topologies, each phase and each cascaded converter are fed-up with an independent source of power (PV + DC/AC converter). On the contrary, in this paper's proposed topology, the three phases of each cascaded converter (DC-AC-AC converter) are fed-up with the same PV array; this is a natural balance due to the magnetic link. Therefore, the problem is reduced to solve the per-cell imbalance. In

reference [100], a power imbalance method was described. This method is based on sharing the cascaded converters' usage equally in the same amount of the imbalance.

The per-cell imbalance occurs when each DC-AC-AC converter's power processes are not equal $(P_{a1} \neq P_{a2} \neq P_{ak})$. The per-cell imbalance affects the DC-link since it is controlled like the average of the k DC-sources; thus, there is no certainty on how each DC-link voltage will react, but a voltage drift of the DC-links will happen, distorting the converter voltage. To surmount the drift problem in the DC-link capacitors, it is necessary to compensate the voltage reference signals v_a, v_b *and* v_c in the modulation stage using a feed-forward mechanism that considers each of the DC-link voltage deviations.

The k DC-link voltages pass through the controller $G_{c1k}(s)$ to perform feed-forward compensation. The controller's output reflects each deviation of the corresponding DC-link voltage from the average reference value. The three-phase voltage reference signals v_a, v_b and v_c are divided by the modified DC-link voltages (V^*_{DCk}) coming from the addition of $G_{c1k}(s)$ with V_{DCk}; as a result, k groups of independent modulation indexes are generated for each of the k DC-AC-AC converters. The changes to the respective modulation indices affect the current that the converter draws from the corresponding DC-link capacitors and thus alter the DC-link voltages. In this way, the k DC-link voltages are regulated to a given reference value (1 kV in the simulations).

The unbalanced situation limits the harmonic components' cancellation in the kth carrier group produced by each cascaded converter; as a direct effect of this dilemma, the V_{PWM} voltage's THD will increase. Consequently, the free zone of switching harmonics is reduced because the most significant harmonic will appear at $2f_c$. Various THD minimization methods have been proposed to extend the free zone of harmonics during unbalanced situations [136-139]. By removing the low-order harmonic distortion found in the unipolar pulse-width carrier frequency, these methods optimize the multilevel converters' switching angles. There are two methods to modulate the carrier signals in CHB converters when unbalanced DC sources or when there is per-cell imbalance due to a partial shading in the PV arrays: symmetric polynomials and resultants and generalized hybrid modulation (GHM) technique [140]. Most of the papers, including a paper published by this author in 2018 [113], use the second approach extending the analyzes for PSPWM, where calculate the proper shifting carrier angles to reduce the THD eliminating the low order harmonics [137].

4.3.5. OPEN-LOOP SIMULATION OF THE THREE-PHASE DC-AC-AC CASCADED CONVERTER

To verify the system's proper operation, some off-grid simulations were done. The purpose of these simulations is to verify the power electronics system's performance and the validation of the proposed converter considering ideal DC power supplies (Figure 4.22). The simulation parameters are in Table 16.

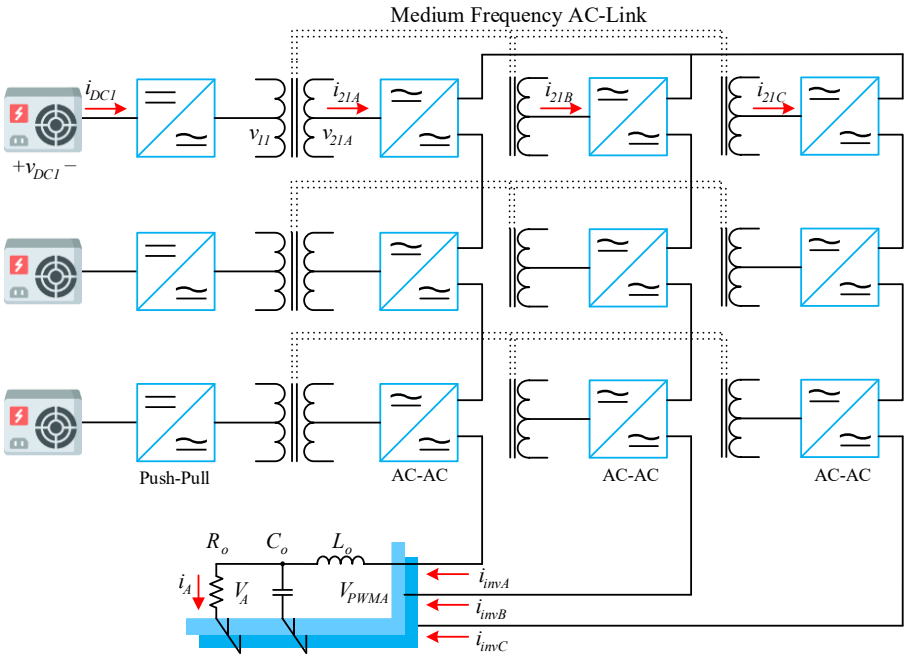


Figure 4.22: Three-phase seven-level DC-AC-AC converter.

Table 16: Simulation parameters for a 3PH 7L DC-AC-AC converter.

Parameter	Acronym	Value
Rated Power	P_o	324.16 kW
Output voltage	V_{LL}	13.20 kV
DC-link voltage	V_{DC}	1.00 kV
Switching frequency	f_{sw}	9.96 kHz
Output levels	m	7
Output frequency	f	60 Hz
Resistive load	R_o	537.52 Ω
Turn ratio	n	4.5
Filter's capacitance	C_o	34.9 nF
Filter's inductance	L_o	20.16 mH
Filter's cutoff frequency	f_{cutoff}	6 kHz
DC link capacitance	C_{link}	6879 μF

As was discussed in section 4.3.2, three cascaded converters are considered. Due to off-grid mode, a resistive load is connected through an inductance-capacitance (LC) filter. The line-to-line voltage is set to 13.20 kV, and the total power output is 324.16 kW. The simulation parameters were obtained in the previous section and are listed in the Table 16. In this simulation, the PV arrays were substituted by ideal power supplies.

Figure 4.23 shows the most representative waveforms in this proposed converter. Figure 4.23 (a) shows the voltage of one of the three DC power supplies. Its value is 1 kV; therefore, the push-pull converter's power switches will block 2 kV; hence, it is recommendable to use switches with a blocking voltage of 3.3 kV. A transformer must be implemented to step up the voltage since the DC voltage should not be higher than 1 kV due to safety and insulation constraints. In this simulation, v_1 is scaled up through the transformer's turn ratio from 1 kV to 4.5 kV; v_{2A}, v_{2B}, and v_{2C} are identical; this is depicted in Figure 4.23 (b), where the medium-frequency square waveforms are presented on the left side, and a zoomed view is shown in the right side.

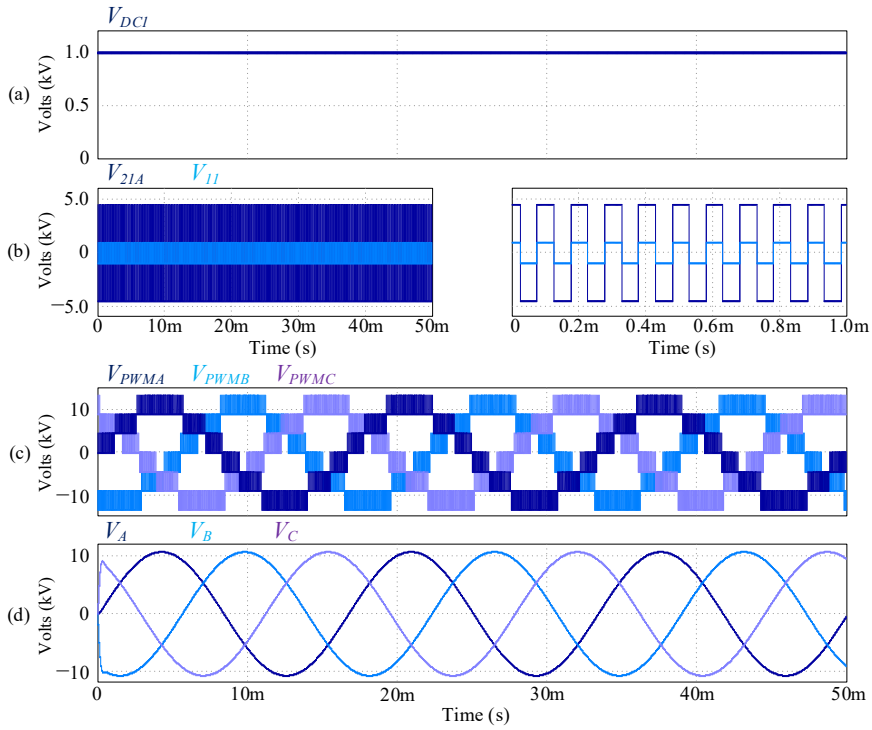


Figure 4.23: Simulation's voltage waveforms. (a) DC source; (b) step-up voltage; (c) multilevel three-phase line-neutral output voltages; and (d) three-phase line-neutral output voltages.

In Figure 4.23 (c), the cascaded three-phase converters generate the seven-level line to neutral voltages in V_{PWM} terminals; their peak voltage reaches 13.5 kV, and the THD is 20.64%. The blocking voltage associated with the AC-AC converter's switches is 4.5 kV; therefore, 6.5 kV IGBT collector-emitter voltage is suitable for this stage [56].

If more DC-AC-AC converters are cascaded, then the voltage rating of the semiconductors will decrease linearly. For example, suppose 3.0 kV devices are used and considering a derating of 50%; in that case, nine cascaded converters will be required to generate a stare output voltage of 13.5 kV peak. Finally, in Figure 4.23 (d), the three-phase sinusoidal line to neutral voltages are present, clearly shifted 120° one after another; the fundamental component is 60 Hz, with a peak value of 10.77 kV. The RMS phase-neutral and line-line voltages are 7.62 kV and 13.2 kV, respectively.

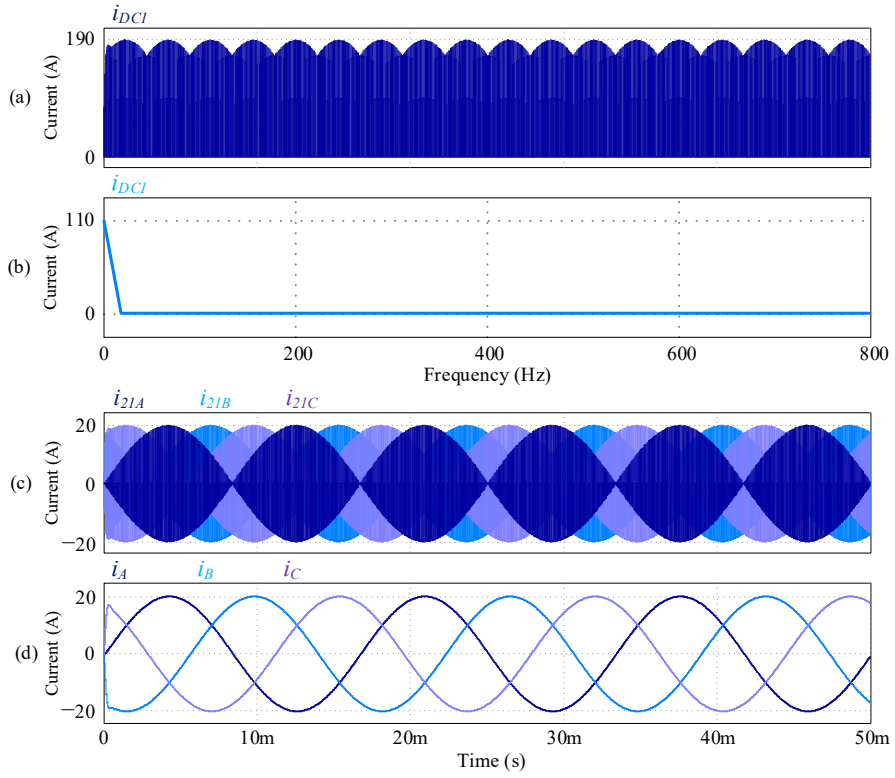


Figure 4.24: Main current waveform for the open-loop simulation. (a) DC source; (b) current harmonic spectrum; (c) current waveform through the secondary windings; and (d) line-output current waveforms.

Figure 4.24 shows the most relevant current waveforms of the converter. Figure 4.24 (a) illustrates the current waveforms in the first DC-link; its average and peak current values are 110.11 A and 191.40 A, respectively.

When the DC link current is seen in detail, the first impression is that there is a harmonic situated at six times the fundamental frequency. However, after verifying the harmonic spectrum in Figure 4.24 (b), it is evident that the DC components are the only low-frequency harmonic. This is supported by the fact that the simulations consider a balanced three-phase system; therefore, the second harmonic current component is canceled via the magnetic link. Thus, the ripple current's shape is only related to the medium-frequency switching harmonics in the power switches.

Figure 4.24 (c) illustrates the secondary windings' current waveforms, one per secondary winding. Its peak current is 20.05 A in any of the medium-frequency transformers. Finally, Figure 4.24 (d) shows the pure sinusoidal current waveform throughout the resistive load; the RMS and peak currents on each phase are 14.017 A, and 20.05 A, respectively.

4.3.6. OPEN-LOOP EXPERIMENTAL RESULTS OF THE THREE-PHASE 3L DC-AC-AC CONVERTER

In order to verify the analysis and simulation results, two reduced versions of a laboratory prototype were built: a five-level single-phase DC-AC-AC converter (Figure 4.25) and a three-level three-phase DC-AC-AC converter (Figure 4.26). These reduced versions focus on validating the proposed topology's conceptual idea. These scaled-down converters are off-grid, and a resistive load is used in the converter outputs after an LC filter.

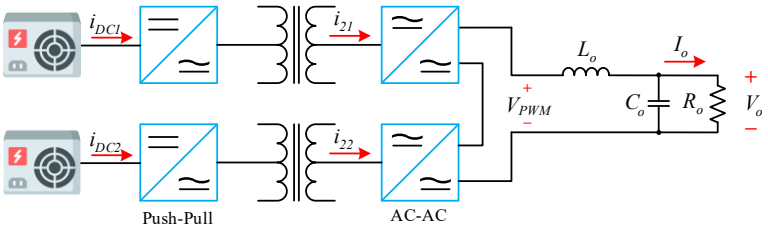


Figure 4.25: Diagram of the five-level singles phase DC-AC-AC converter.

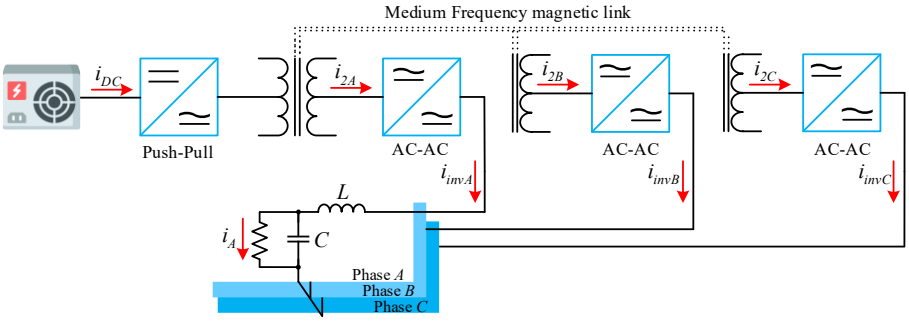
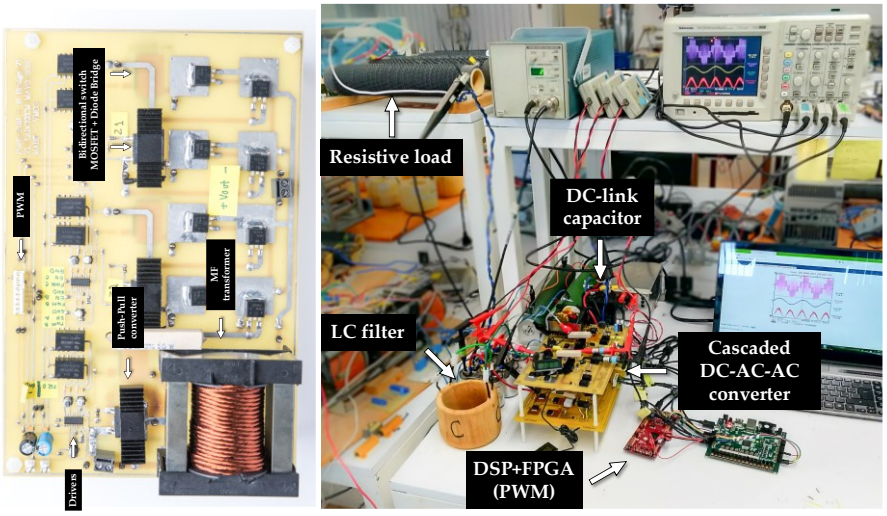


Figure 4.26: Diagram of a three-level three-phase DC-AC-AC converter.

4.3.6.1 Single-phase five-level DC-AC-AC converter in open-loop

The first reduced version consists of two cascaded DC-AC-AC converters; the diagram is shown in Figure 4.25. A single-phase DC-AC-AC converter (Figure 4.27) is built with six IXTT69N30P MOSFETs (Littelfuse), two for the push-pull converter and four for the AC-AC converter.



(a) (b)

Figure 4.27: (a) Photography of the actual printed circuit board (PCB) for the single-phase five-level DC-AC-AC converter. (b) Photography of the actual setup for the single-phase five-level DC-AC-AC converter.

Each switch in the AC-AC converter is integrated by a MOSFET and a diode bridge which gives the feature of a bidirectional switch. Four 15ETH03 diodes (Vishay, Malvern, United States) were selected for the diode bridge. An ETD-59 transformer

core (TDK Corporation) with N97 material was selected for the medium-frequency transformer. Switching signals are generated in a TDSM28F379D DSP (Texas Instruments Incorporated, Dallas, United States) and post-processed for the switching strategy in an FPGA Nexys 4 (Digilent, Pullman, United States).

The parameters of the single-phase DC-AC-AC converter are the following: output RMS voltage V_o = 127 V; input voltage DC source V_{DC} = 120 V; switching frequency f_{sw} = 9.960 kHz; line-frequency f_o = 60 Hz; output inductance L = 1.8 mH; output capacitance C = 3.5 µF; resistive load R = 20 Ω; transformer's turn ratio n = 2; and modulation index m_a = 0.75.

Figure 4.28 exhibits the most representative voltage waveforms of a single cell. Channel (Ch) 2 illustrates the square MF AC voltage v_1 of the transformer's primary winding; the duty cycle of v_2 is 50%. Ch3 shows the voltage v_2 in the transformer's secondary winding, the voltage of v_2 is n times v_1. Finally, Ch4 depicts the three-level voltages in V_{PWM} obtained due to the unipolar SPWM modulation technique; its amplitude is directly related to the voltage present on v_2.

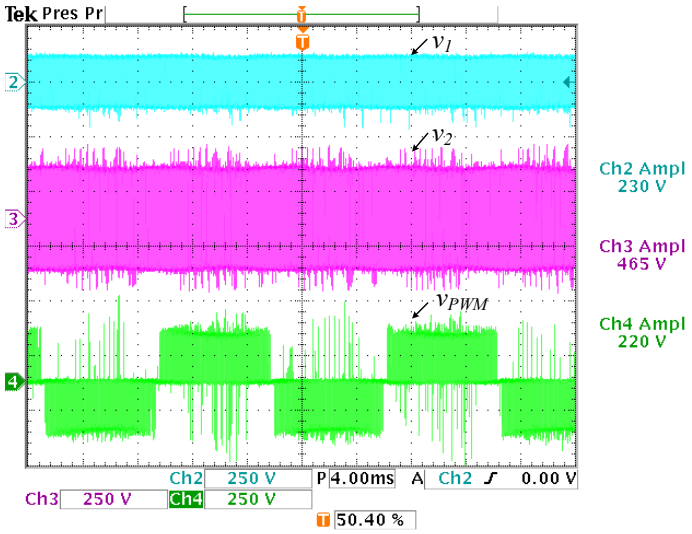


Figure 4.28: Main voltage waveforms in a single cell: Ch2 primary winding voltage, Ch3 secondary winding voltage, Ch4 V_{PWM} voltage.

The main current waveforms are in the oscilloscope's screenshot in Figure 4.29. Ch2 shows the current i_{DC} in the DC link; this current is the same that is flowing through the MF transformer's central tap. The shape of the current waveform of i_{DC} is practically the same as the DC-link current in a two-level inverter. The average and peak currents of i_{DC} can be calculated according to Equations (4.8) and (4.9). In contrast with the simulations where no over-shoots were presented, the MF

transformer's central tap current shows overshoots of approximately 20% in the experimental results. Ch3 displays the current i_2 in the MF transformer's secondary winding; its RMS value is 4.16 A. Ch4 reveals the current i_o that flows in the resistor its RMS, and peak values are 6.26 A and 8.85 A, respectively.

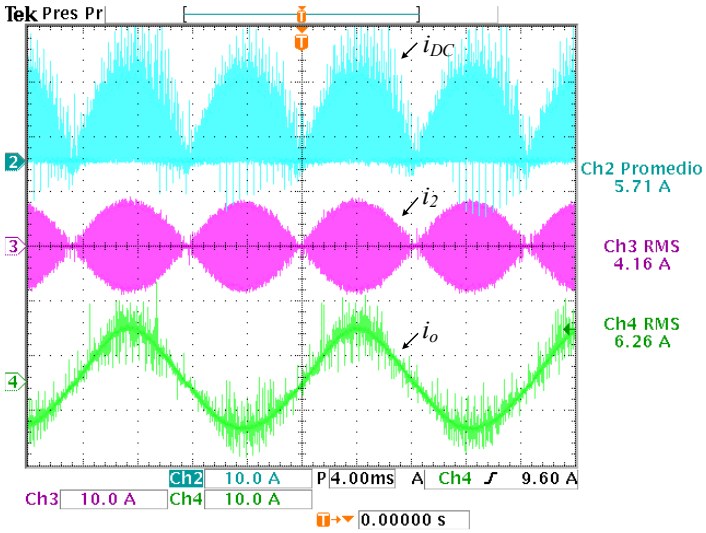


Figure 4.29: Main current waveforms in a single cell: Ch2 current in the DC-link, Ch3 secondary winding current, Ch4 resistor's current.

Table 17: Five-level single-phase DC-AC-AC converter's parameters.

Parameter	Acronym	Value
Output voltage	V_{LL}	203 V
DC-link voltage	V_{DC}	120 V
Modulation index	m_a	0.6
Switching frequency	f_{sw}	9.96 kHz
Output levels	m	5
Output frequency	f	60 Hz
Transformer truns ratio	n	2
Inductance	L	1.8 mH
Capacitance	C	2 uF
Resistance	R	30 Ω

Regarding the single-phase multilevel configuration, Figure 4.27 (b) is the actual setup's photography; Table 17 shows the setup's parameters. Figure 4.30 shows the main experimental results based on the multilevel configuration; two cascaded 1PH DC-AC-AC converters are used to generate the five-level output voltage. Ch3 shows the five-level output voltage V_{PWM} with an approximate amplitude of 480 V. Ch4 is the output voltage after the LC filter, with a RMS value of 207 V. The voltage spikes in the total V_{PWM} terminals are generated due to the delivery of the energy of the MF transformer's leakage inductance when the current path is broken due to the hard-switching commutation in the matrix converters. Ch1 reveals the RMS current on the resistive load; its RMS value is 7.49 A. Finally, the mathematical channel indicates the output power measured in the resistive load, and its value is 1.54 kW, (770 W per converter).

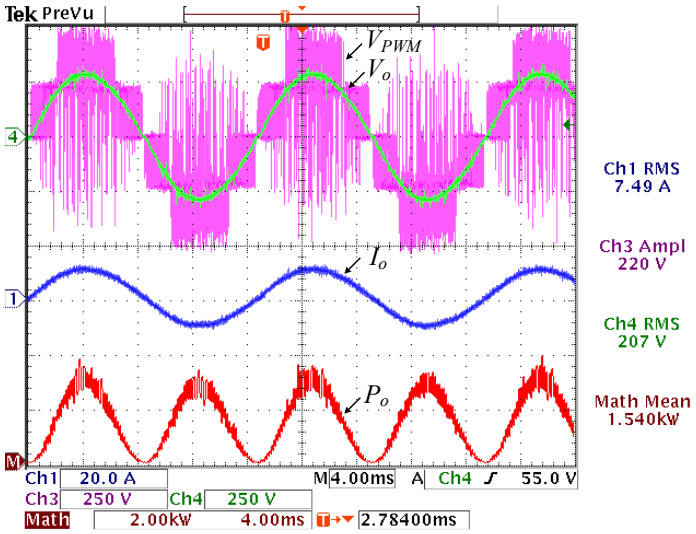


Figure 4.30: Experimental results of the 5L single-phase DC-AC-AC converter. Ch3 and Ch4 are the output voltages before and after the LC filter. Ch1 is the output current through the resistive load. The mathematical channel (ChMath) is the mean output power.

Figure 4.31 presents more experimental results in the multilevel configuration. In this scenario, one of the two cascaded DC-AC-AC converters is inactive, while the other is active. Considering that each division represents 4 ms, the second DC-AC-AC converter is turned on t = 18 ms. The introduced perturbation does not generate any disturbing voltage or current overshoot as seen in the waveforms. Ch1 presents the current in the resistive load; its peak value changes from 9.40 A to 18.60 A. Ch3 illustrates the voltage before the LC filter; its waveform changed from three levels (with a peak value of 239.80 V) to five levels (with a peak value of 479.10 V) after the second converter was turned on. Ch4 depicts the output voltage after the LC filter; the peak voltage changed from 141.00 V to 294.00 V.

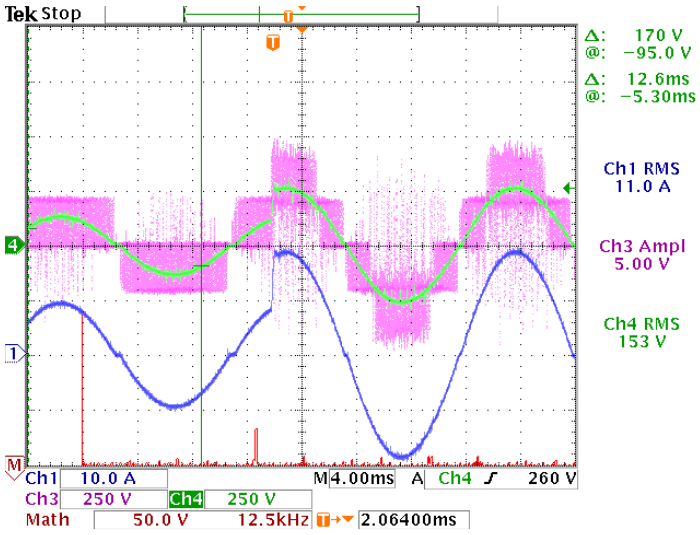


Figure 4.31: Experimental results on multilevel configuration, Ch3 and Ch4 are the output voltage before and after the LC filter, respectively, and Ch1 is the output current through the resistive load.

4.3.6.2 Three-phase three-level DC-AC-AC converter in open-loop

Figure 4.32 (a) shows the second reduced version of the experimental prototype consisting of one DC-AC-AC converter in a three-phase configuration; the block diagram is shown in Figure 4.26.

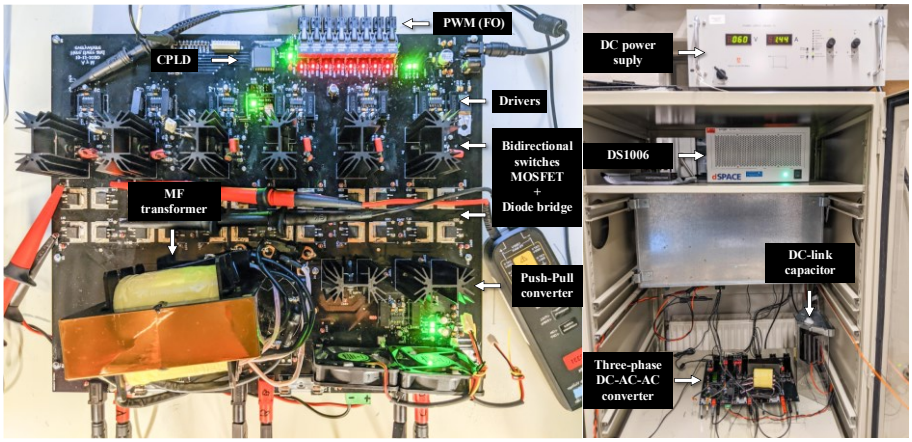


Figure 4.32: Photographs of the actual setup for the three-phase three-level DC-AC-AC converter: (a) PCB of the three-phase DC-AC-AC converter; (b) Setup for the three-phase DC-AC-AC converter (from top to bottom: DC-power supply, dSPACE).

The 3PH DC-AC-AC converter is assembled with four IXTH36N50P MOSFETs (Littelfuse) per phase for the AC-AC converter and two IXFK100N65X2 (Littelfuse) integrate the push-pull converter. The bidirectional switches are integrated in the same way that in the first reduced version. An EE 110/36 transformer core (TYDZ) with PC40 material was selected for the medium-frequency transformer.

The modulation strategy was generated in the dSPACE environment through a DS1006 processor accompanied by a DS5203 board (dSPACE GmbH, Paderborn, Germany). The processor and the FPGA share data according to Figure 4.33. The DS1006 board generates a modulation index that is sent to the FPGA by a data write block; then, the data is interchanged with the FPGA through the "load BUS". Then, the FPGA reads that data by a data read block. Later, this data is compared with a counter by a comparator block, and its output is the PWM that is sent to the power converter by fiber optic. The FPGA was programmed with the RTI FPGA Programming by Xilinx System Generator Simulink blockset. Figure 4.34 shows a connection diagram of how the power converter is interfaced with the dSPACE system, and the actual setup used for this experimental part (Figure 4.32).

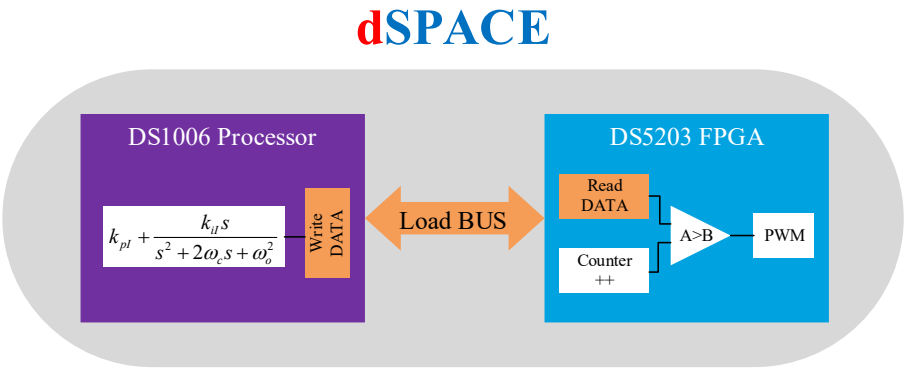


Figure 4.33: Data exchange between the processor and the FPGA.

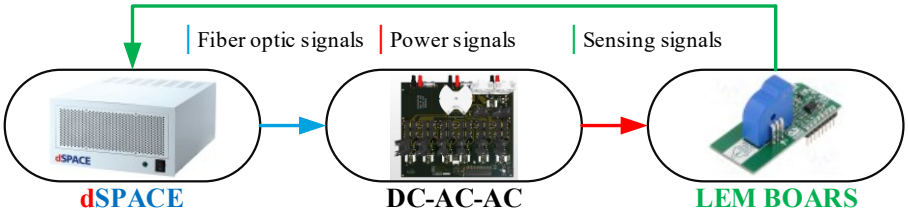


Figure 4.34: Diagram connection of the power converter and the digital system.

This converter was designed considering that it will be part of a 3PH-7L DC-AC-AC converter. The parameters of the converter are in Table 18.

Table 18: Three-phase DC-AC-AC converter's parameters.

Parameter	Acronym	Value
Output voltage	V_{LL}	170 V
DC-link voltage	V_{DC}	120 V
Modulation index	m_a	0.85
Switching frequency	f_{sw}	10 kHz
Output frequency	f	50 Hz
Transformer turns ratio	n	1.34
Inductance	L	1.8 mH
Capacitance	C	27 uF
Resistance	R	30 Ω

Figure 4.35 presents the waveforms generated by phase A of the three-phase DC-AC-AC converter. Ch1 illustrates the current through the resistive load of phase A; its RMS value is 136.0 mA. Ch3 and Ch4 are the line to neutral output voltages of V_{PWMA} and V_A. Their amplitudes are 45.0 V and 90.0 V, respectively. Both voltages are measured before and after the LC filter. Figure 4.36 depicts the line-to-line V_{PWM} output voltages before the LC filter, its shape has five levels as expected, and the peak-to-peak voltage for each phase is 360.0 V. The subsequent two figures represent the line-to-line voltages and currents in the converter. The line-to-line voltages are measured after the LC filter; therefore, the waveforms are purely sinusoidal. The results are shown in Figure 4.37; the peak-to-peak and the RMS values are 380.0 V and 97.1 V, respectively. Finally, Figure 4.38 shows the three-phase output currents with an RMS value of 2.98 A. As was expected, the waveforms are completely sinusoidal; they show a peak value of 4.12 A.

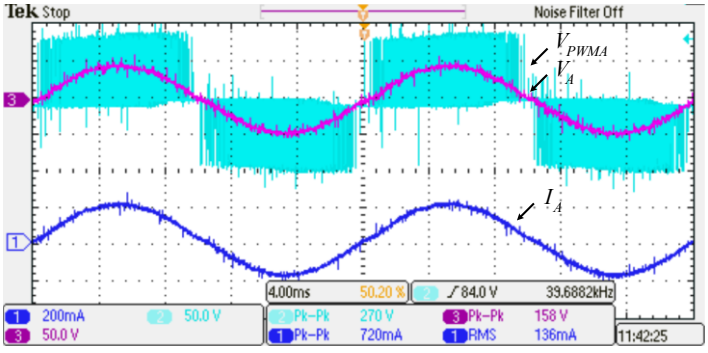


Figure 4.35: Waveforms generated in phase A of the three-phase DC-AC-AC converter. Ch1 Output current, Ch2 Line to neutral output voltage before filter, Ch3 Line to neutral output voltage after filter.

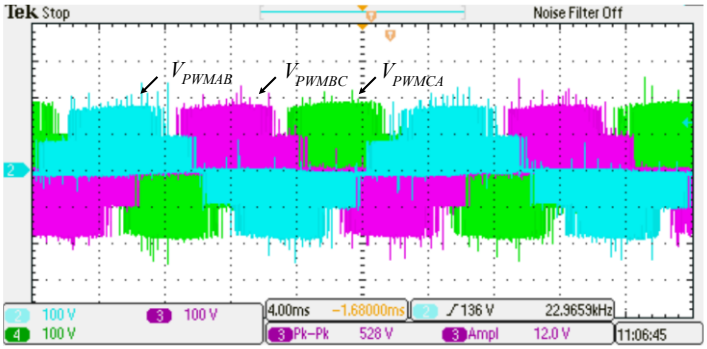


Figure 4.36: Waveforms of the three-phase DC-AC-AC converter; line-to-line voltages (V_{PWM}) before the filter, Ch1 Phase AB, Ch3 Phase BC, Ch4 Phase CA.

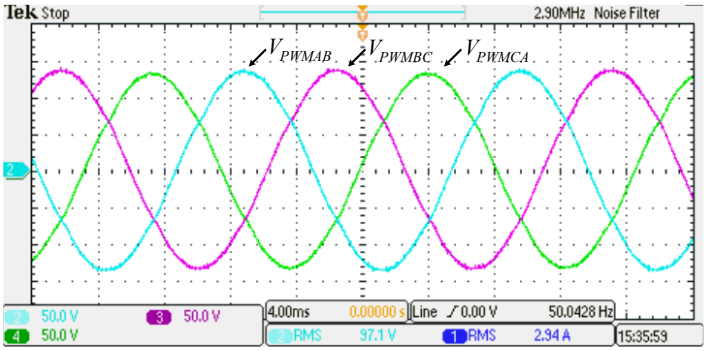


Figure 4.37: Line to line voltages (V_{LL}) after the LC filter. Ch2 Phase AB, Ch3 Phase BC, Ch4 Phase CA.

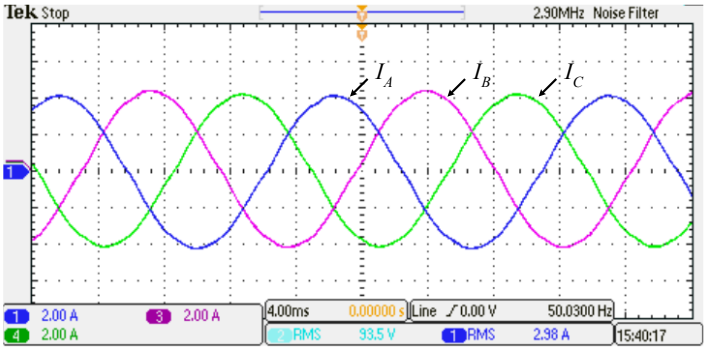


Figure 4.38: Output currents through the three-phase resistive load. Ch1 Phase A, Ch2 Phase B, Ch3 Phase C.

4.3.7. CLOSED-LOOP HARDWARE IN THE LOOP RESULTS IN THE THREE-PHASE 3L DC-AC-AC CONVERTER

Nowadays, there is a high level of confidence with a good understanding of how mathematical model behaves. In the same sense, today, it is possible to represent physical components like cables, machines, passive elements, and even semiconductors with optimal fidelity under certain conditions. Therefore, it is possible to simulate the power plant on a real-time platform and keep the controller under test intact on real hardware like a microcontroller or a DSP. This concept is called Controller Hardware In the Loop (C-HIL). And this is what is done in this section.

The connection diagram of the Rapid Control Prototype (RCP) dSPACE platform and the Real-Time (RT) Typhoon HIL simulator are depicted in the figure below. The dSPACE system is in charge of running the control laws, signal acquisition and PWM generation. The processor runs the control laws at 10 kHz, the FPGA generates the PWMs at 10 kHz, and the plant (the power electronic converter) is running on the Typhoon HIL at 200 Mhz.

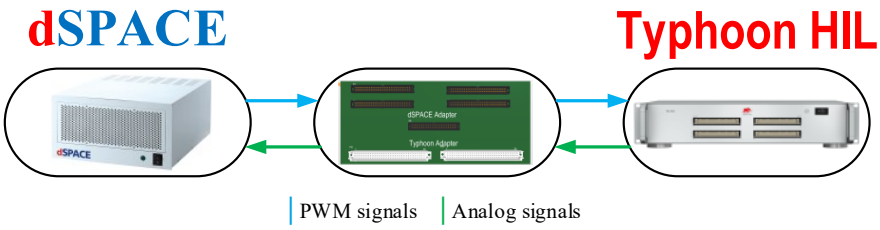


Figure 4.39: Connection diagram of the power converter simulated on an RT simulator and the RCP platform.

The power plant consists of a three-phase DC-AC-AC converter fed by a DC power supply; the converter is connected to a local load through an LC filter. The load is resistive, but additionally, a nonlinear load can be added if the respective contactor is closed. The detailed plant model is shown in Figure 4.40. The root model of the Simulink controller is depicted in Figure 4.41. A brief description is given next.

The controller (Figure 4.41) consists of several subsystems, each in charge of a different task. The upper left blue square represents the controller gains, these are constant blocks, but once the system is running, the user can modify them online through the Control Desk software that can read or write any data buffer on the dSPACE system. The bottom left orange square represents the measurements on the system; this block gets, for example, capacitor voltages, inductor currents, and the DC power supply voltage. All these measurements take place on the FPGA and are later transferred to the LOAD BUS to reach the processor finally.

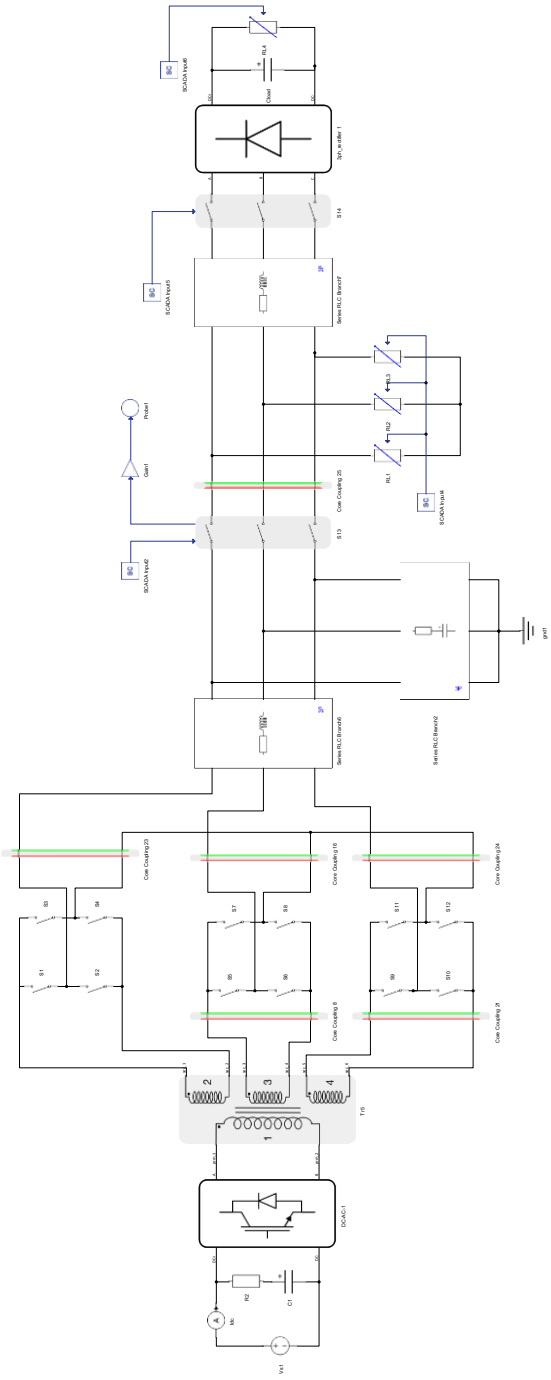


Figure 4.40: Power plant modeled in Typhoon HIL.

The yellow box (INVERTER I CONTROL) contains the controller, where the voltage and current control loops operate in a cascaded way. The green box represents the modulation stage. Finally, the red square represents the data transfer boxes. These boxes take the information generated by the DS1006 processor and send it to the FPGA. Basically, the only data that is being transferred from CPU to FPGA are the modulation indices. More detail about the FPGA block (a grey block at the bottom left of the figure below) is found at Appendix A.

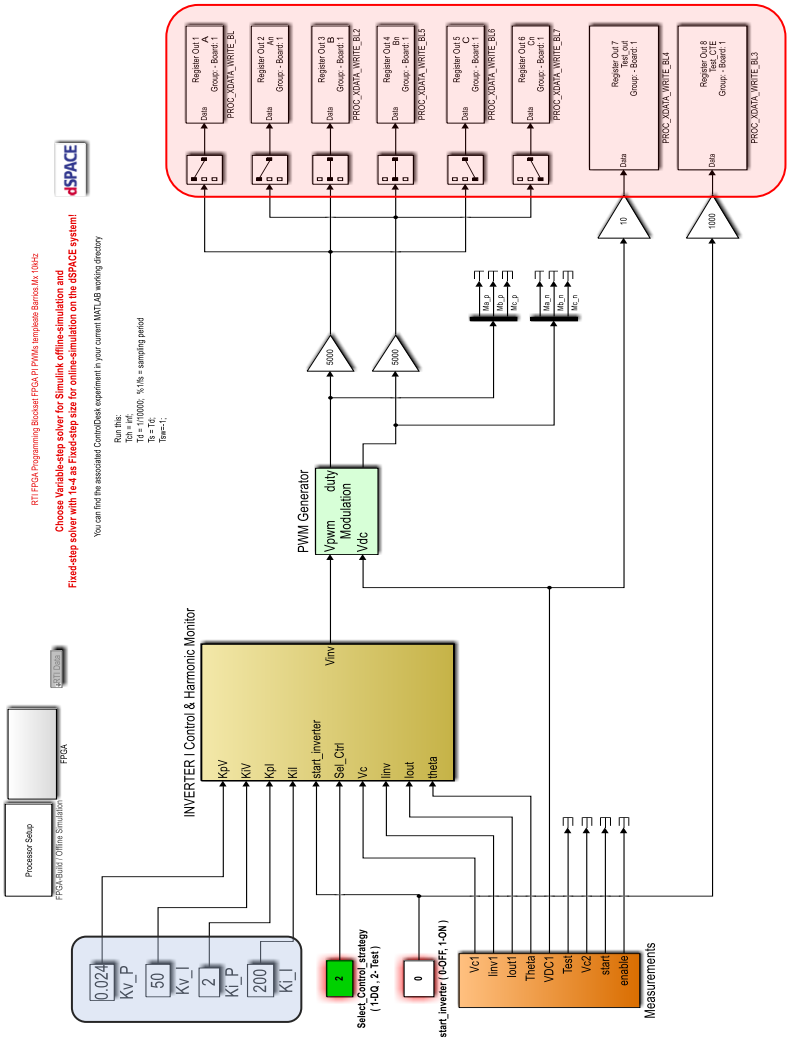


Figure 4.41. Simulink root control model.

The following two figures, Figure 4.42 and Figure 4.43, respectively, show the SCADA panel of each environment (Control Desk and Typhoon HIL SCADA). Because the controller is running on the dSPACE system, its variables (controller gains) can be modified only at the Control desk. Nevertheless, it can show the sensed variables like capacitor's voltages, inductor's currents, DC link capacitor voltage, and even the internal variables of the controller, for example, modulation indices or error signals. On the other hand, Typhoon HIL SCADA can display all the sensed variables using the virtual oscilloscope tool. From this SCADA panel, the user can interact with the system by changing the plant parameters utilizing the input controllers.

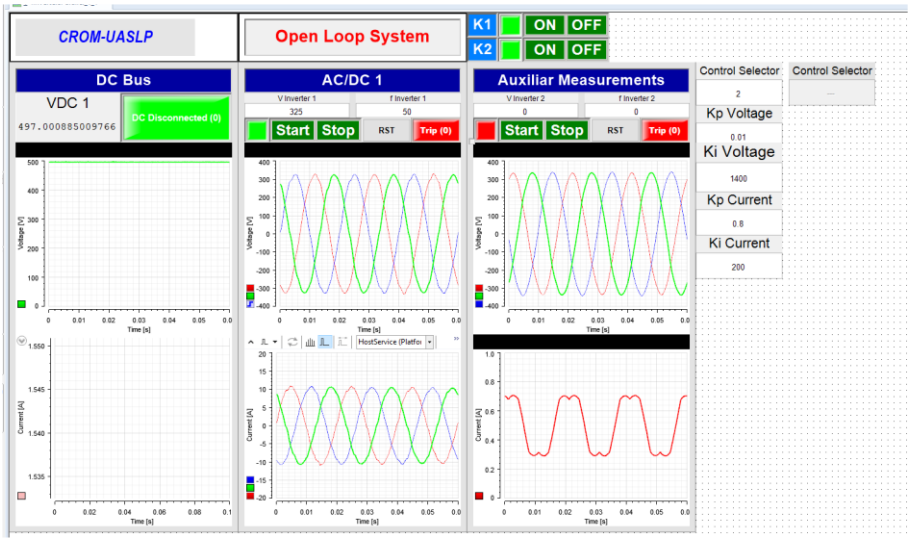


Figure 4.42: Control Desk, SCADA Panel.

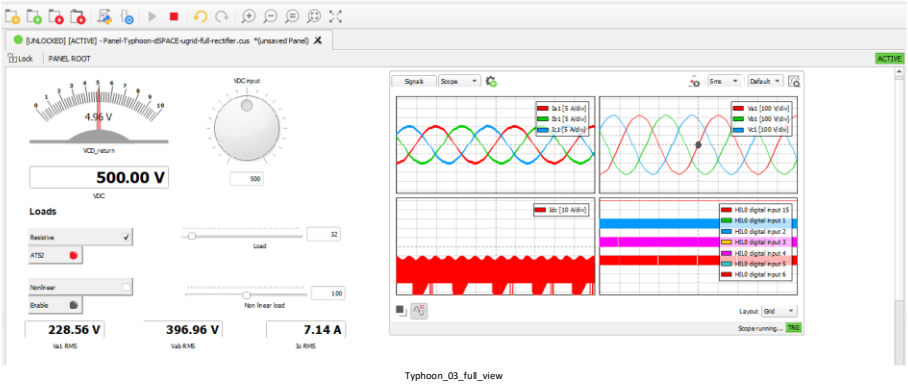


Figure 4.43: Typhoon HIL Control Center, SCADA Panel.

4.3.7.1 C-HIL Results: step load

For the C-HIL results, the most representative parameters of the power plant are given in Table 19. The tests are done in order to verify that the power converters (specifically the internal controllers) do not get unstable perhaps the unexpected changes in the load, input voltage, output, voltage, or nonlinear loads.

Table 19: Power plant parameters for C-HIL results.

Parameter	Acronym	Value
Output voltage	V_{LL}	400 V
DC-link voltage	V_{DC}	650 V
Switching frequency	f_{sw}	10 kHz
Output frequency	f	50 Hz
Transformer turns ratio	n	1.34
Inductance	L	8.6 mH
Capacitance	C	9 uF
Resistance	R	16 Ω
Voltage proportional gain	k_{pV}	0.01
Voltage resonant gain	k_{iV}	7.45
Current proportional gain	k_{pI}	25

Figure 4.44 shows a change in the load; in this scenario, the controller reference is set to 325 V (peak capacitor's voltage phase-neutral). Two sets of waveforms integrate the figure; the top set is the three-phase capacitor's voltage waveforms, while the bottom set is the three-phase inductor's current.

The test starts at $t = -0.1\ s$ with a resistive load of 32 ohms per phase, the capacitor's peak voltage is 325 V, and the inductor's peak current is 10 A. During this interval, the voltage and current waveforms look somehow distorted; therefore, the THD_v is verified; it is 3.2%, a value that is within the 5 % limit. At approximately $t = 0$ s, the resistive load decreases to 16 ohms per phase, which is translated into an increase of current from 50 % of the rated current to 100 %, in other words, from 10 to 20 A peak. There is an overshot in the voltage, and in the current waveform, the overshot is around 15% of the final value and its duration is below 100 ms. At full load, the THD_v improves from 2.6 % to 1.5 %.

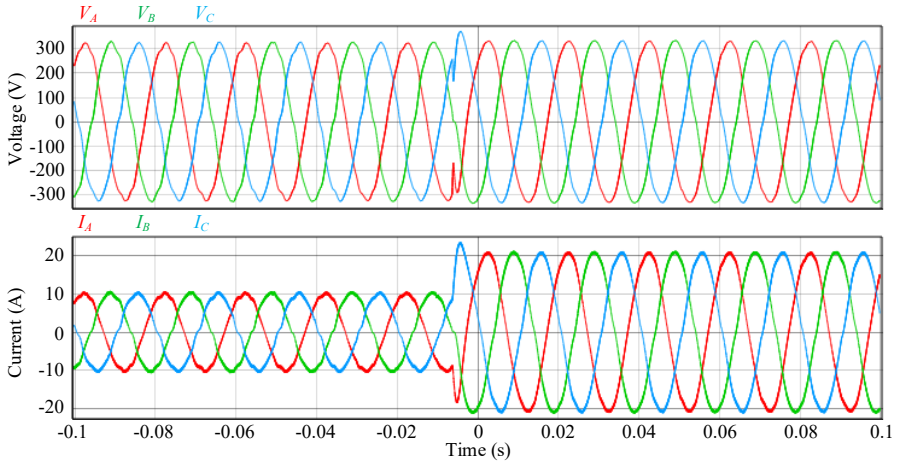


Figure 4.44: Step load change from 32 ohms to 16 ohms.

4.3.7.2 C-HIL Results: Output voltage step

For the following scenario, a voltage reference step is performed in order to test the stability of the converter under such scenario. The capacitor's phase-neutral peak voltage reference changed from 179.62 V to 326.59 V, which is translated to phase-to-phase voltage from 220 V to 400 V. To visualize the transitory on the waveform (Figure 4.45), the capture period was increased to one second. As seen in the figure, the transitory last 300 ms. After the voltage step change, the peak current changes from 11.11 A to 20 A.

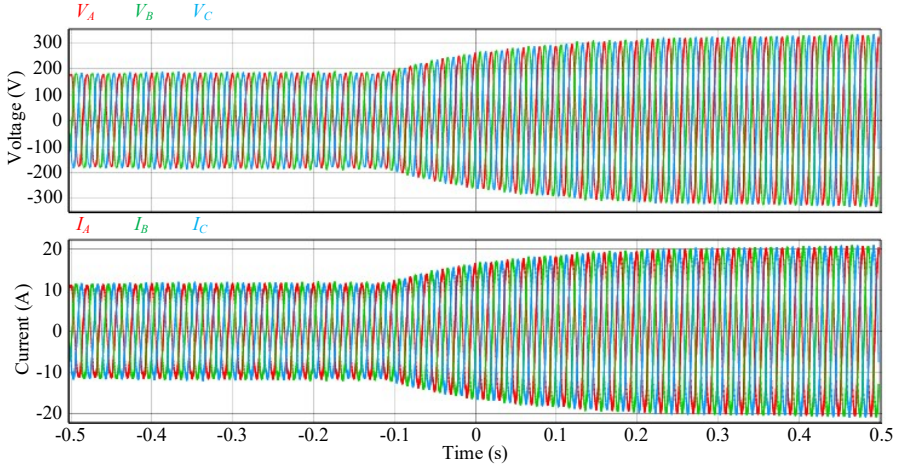


Figure 4.45: Step voltage reference change from 180 to 325 V.

4.3.7.3 C-HIL results: non-linear load

A nonlinear load is connected to the DC-AC-AC converter for the following scenario. This test will ensure that the controllers, perhaps the nonlinear load, keep the power plant stable. For this test, the contactor S14 of Figure 4.40 is kept close during the whole test. The nonlinear load is modeled as in the figure below (Figure 4.46); it is a three-phase, six-pulse, full-bridge diode rectifier, which is a typical configuration implemented to rectify three-phase voltages [141]. The non-linear load is interfaced with the DC-AC-AC converter by an inductor (L_s = 1 mF), and it serves as an additional load to the resistive baseline load. A filter capacitor (C = 235 µF) in parallel to the DC side is used to filter the current that is injected into the resistive load (R_l = 100 Ω). Then, the effect of the connection of such nonlinear load to the DC-AC-AC converter is examined in this section.

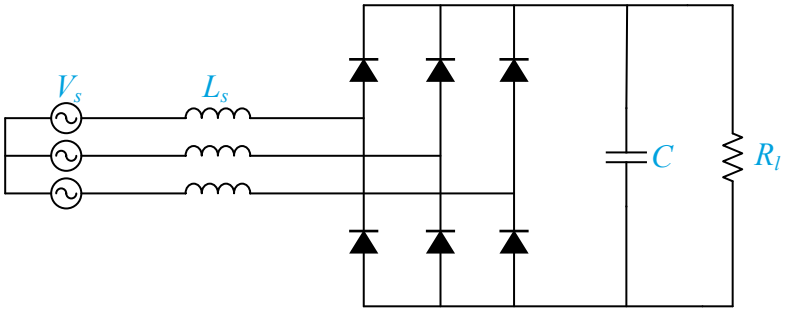


Figure 4.46: Three-phase six-pulse rectifier as a load for the DC-AC-AC converter.

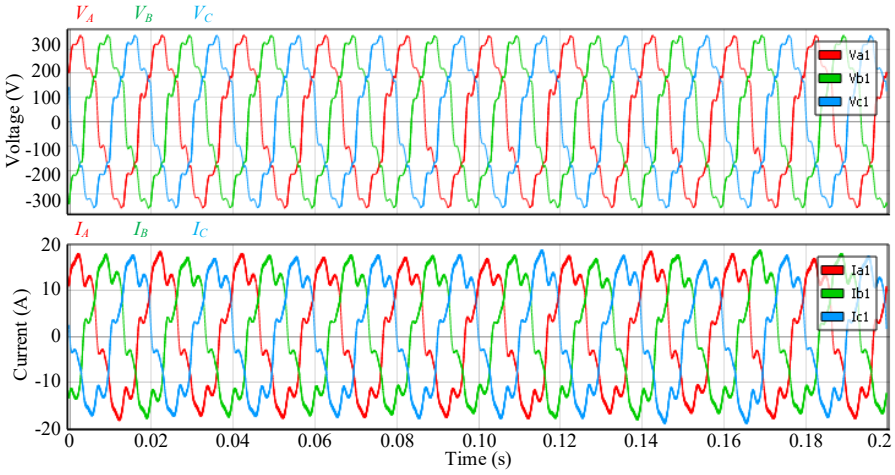


Figure 4.47: Voltage and current waveform with a nonlinear load.

Due to the high value of the inverter's inductor and that the controller was not designed to cope with nonlinear loads up to this point, neither the modulation (for example selective harmonic elimination), the behavior of the voltage and current waveform (Figure 4.47) is different from what is expected from a setup as in Figure 4.46.

The voltage waveforms (V_A, V_B, V_C) of the previous figure are stable but contains harmonic content (see Figure 4.48) due to the controllers have not considered yet harmonic compensation, refers to section 4.3.3.5; in the aforementioned section, the voltage controller only acts on the fundamental harmonic, while the voltage controller's bandwidth is limited to 262 Hz. The voltage reference is kept as in the previous section (325 V), and the output voltage is 402 VRMS with a THD of 12 %. In this case, the 5th, 7^{th,} and 11th are the most affected by the non-linear load. For the current waveforms, the conclusions are similar, their RMS value is 12 A, and there is harmonic content especially on the 5th and 7th order harmonics, the total THD for the current is 21 %.

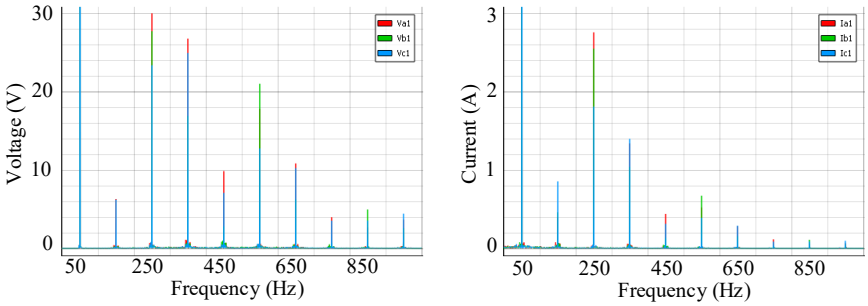


Figure 4.48: FFT of the waveform of Figure 4.47.

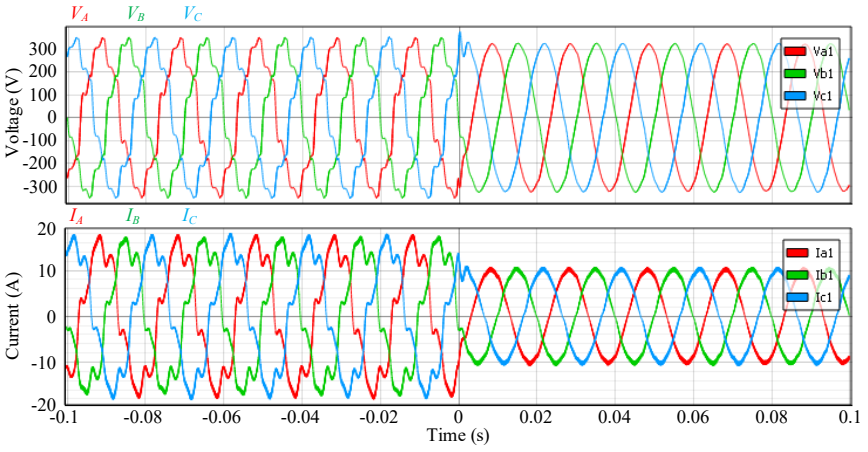


Figure 4.49: From nonlinear to linear load test.

In the following test (Figure 4.49), the nonlinear load is removed at $t = 0$ s. The control system recovers almost instantly. The output waveform (voltage and current) is now free of the harmonic content while the system remains stable. The following scenario (Figure 4.50) presents the voltage and current behavior once the harmonic compensator (HC) controllers Eq. (4.30) are activated for the voltage loop. In this case, the 5th, 7th and 11th harmonics are compensated in the voltage controller. The new THD for the voltage and current waveforms are 4.2 % and 22 %, respectively. The FFT of these waveforms is depicted in Figure 4.51. As seen in this figure, the harmonic content of the 5th, 7th, and 11th are drastically reduced.

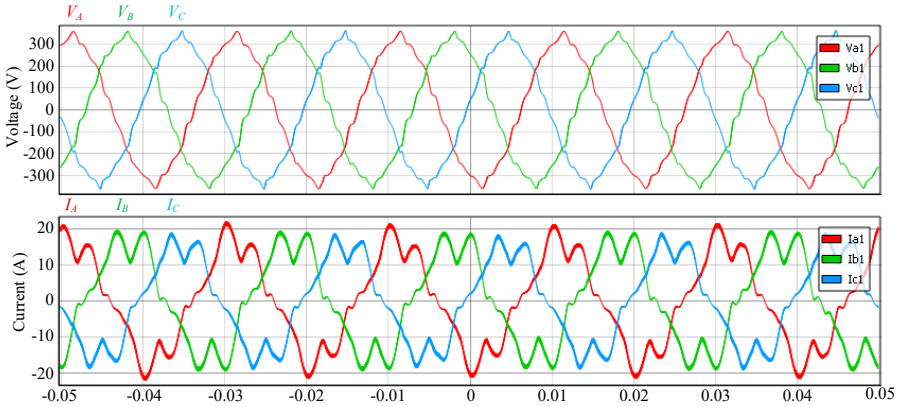


Figure 4.50: Capacitor's voltage and inductor's current waveform with HC.

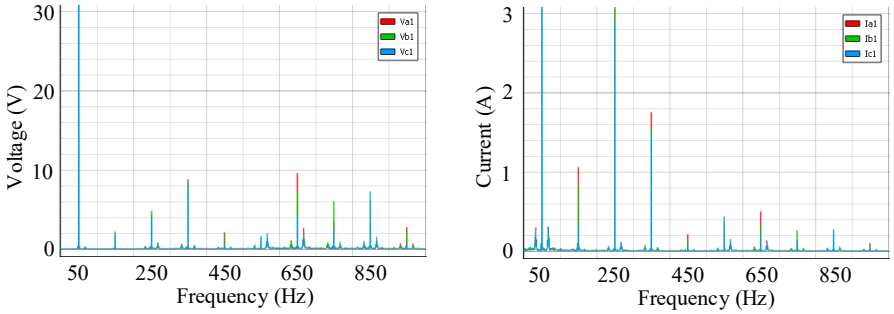


Figure 4.51: FFT of the waveform of Figure 4.50.

Finally, the last test in this section is related to activating the harmonic compensators in the voltage loop. This is done from the SCADA panel designed in the Control Desk. Then the voltage and current response is captured in Typhoon-HIL's scope. As seen in Figure 4.52, the HC is activated at $t = 0$ s, and the voltage's transitory last 40 ms. In contrast, the current's transitory lasts one fundamental cycle, the steady-state is achieved, and the system stays stable.

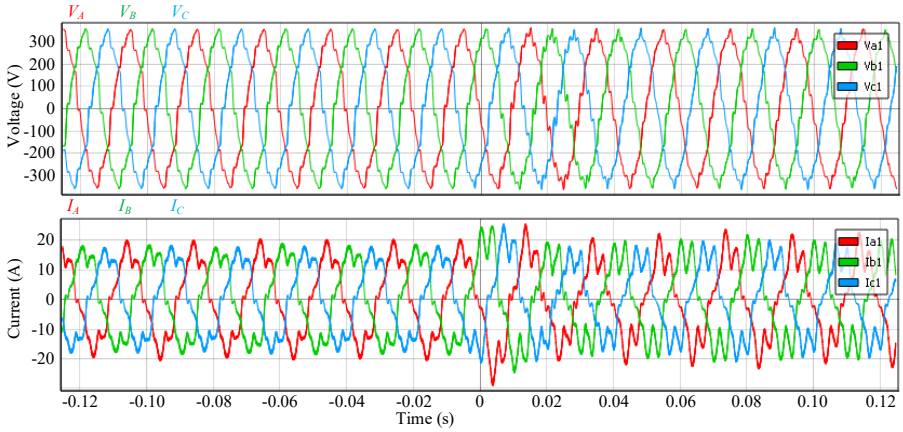


Figure 4.52: Transition between the voltage controller without HC to the voltage controller with HC.

4.3.8. CLOSED-LOOP EXPERIMENTAL RESULTS OF THE THREE-PHASE DC-AC-AC CONVERTER

Once the controller was verified previously in the C-HIL tests, it is now tested on the experimental setup of section 4.3.6.2. The hardware difference between the open-loop and the closed-loop experimental test is the addition of the sensing stage. The sensed variables are the filter capacitor's voltages, the filter inductor's current, and the DC-link voltage. The LEM board measures these power signals (Figure 4.53) and feedback to the dSPACE system by the DS2004 ADC board. The digital acquisition values are brought back to the control system by the ADC read block from the dSPACE system library. The last step is to scale the digital acquisition value to the real magnitude.

Two scenarios are tested to verify the performance of the closed-loop experimental validation. In the first test, a step-change in the reference voltage is made, the initial peak voltage is 50 V, and the new reference is 100 V. In this case, the load is resistive with a value of 460 Ω. The main results are displayed in Figure 4.54. Ch1, Ch2, and Ch3 are the corresponding phase to neutral capacitor's voltage, and Ch4 is the current through the inductor. The transitory time is 400 ms, and there is no overshoot either in the voltage or the current waveform.

The second test (see the results in Figure 4.55) is a step-change in the resistive load. In this experiment, the resistive load is reduced from 460 Ω to 110 Ω in each phase, translated into a step current from 200 mA to 1000 mA. The transitory presents a fast oscillation (2 ms) due to the mechanical switch that was used for the test. The duration of the transitory is 12.5 ms. After the transitory, the converter remains stable, perhaps the load disturbance.

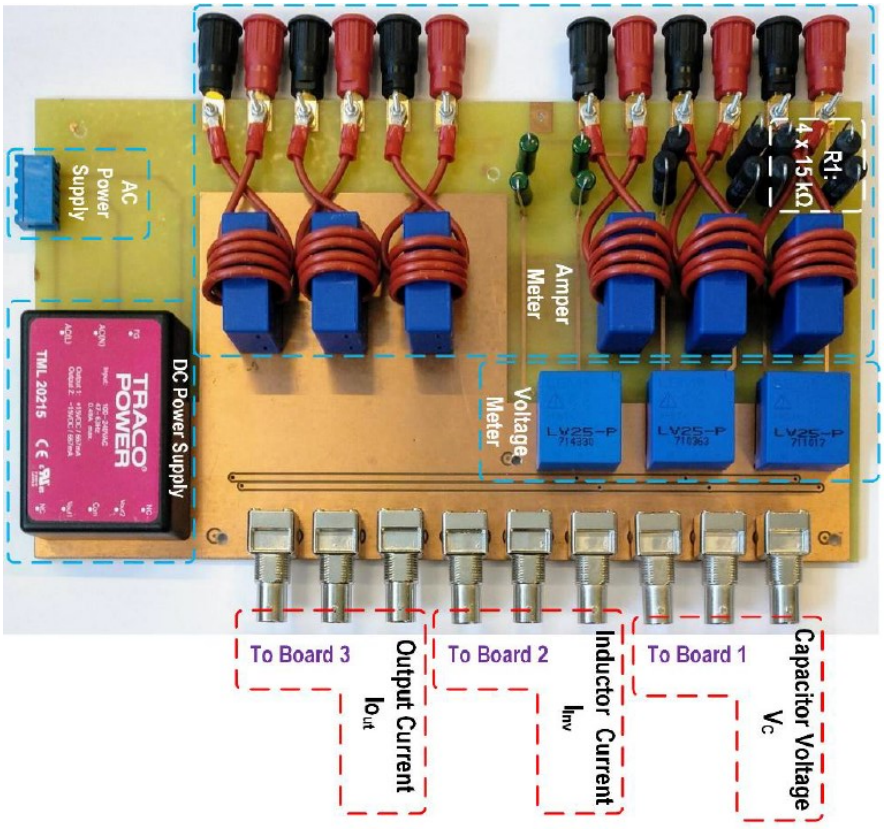


Figure 4.53: Sensing stage for the closed-loop experimental validation.

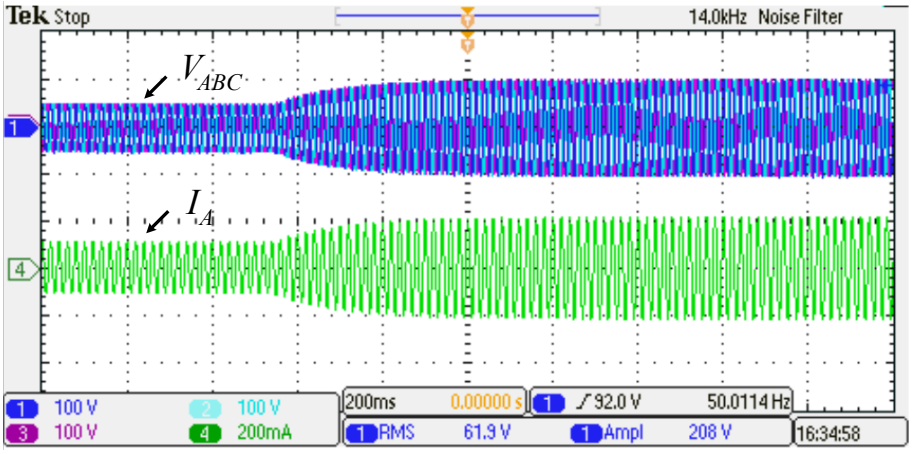


Figure 4.54: Closed-loop experimental results, voltage step-change.

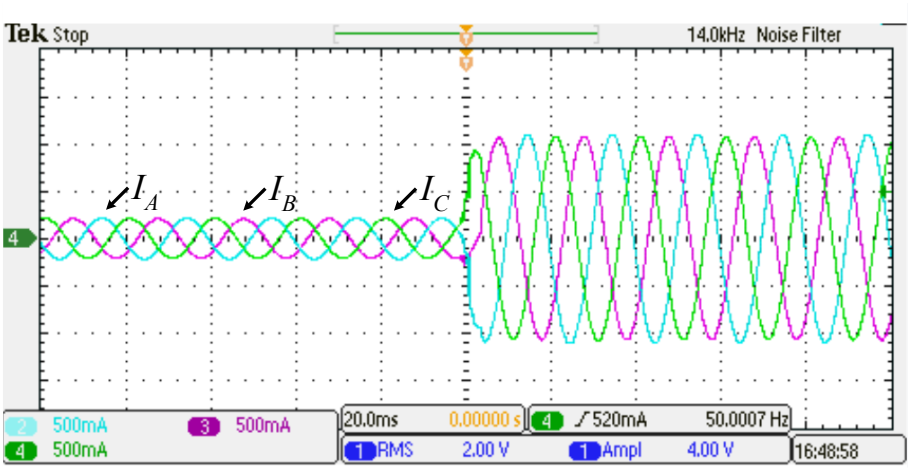


Figure 4.55: Closed-loop experimental results, load step-change.

4.3.9. CLOSED-LOOP SIMULATION OF THE THREE-PHASE SEVEN-LEVEL DC-AC-AC CONVERTER

The subsequent simulations (Figure 4.56 and Figure 4.57) use an SW250poly PV module (SolarWorld, Bonn, Germany); the main parameters of the PV module are: cells per module are 60; the voltage at maximum power (V_{mpp}) is 30.8 V; current at maximum power (I_{mpp}) is 8.12 A; maximum power (P_{max}) is 250 Wp. Therefore, 2000 cells are considered to reach 1000 V, and thirteen PV modules parallel integrate the PV-array. The DC-link voltage reference is 1000 V; the grid's line-to-line RMS voltage is 13.20 kV. The grid's interconnection is through an LC filter, which values are 60 mH, 100 nF, respectively. The grid impedance is taken into account in this simulation, considering that the short-circuit current is 7.05 kA and a X/R ratio of 5. The resulting grid inductance and resistance are found on Table 20.

In Figure 4.56, the most representative waveforms of the simulation are drawn as follows. (a) DC-link voltages; (b) power available versus power generated in the PV; (c) PV currents. This scenario is described as follows; the light intensity for the three PV-arrays is 1000 W/m^2 for the time t interval given in seconds s, $0 \leq t < 0.1$ s; this means that the voltages' values, powers, and currents remain equal in any of the three sets. The magnitude of three DC-links voltages, the available and the harvesting powers, and the currents are 1 kV, 108.05 kW, and 108.05 A, respectively.

First, the DC-links voltages got an overshoot; the maximum overshoot belongs to V_{DC1} = 1009.51 V, with a settling time of 55.5 ms. Second, each PV-array's available power decreased from 108.05 kW in every PV-array to 74.16 kW, 51.57 kW, and 40.28 kW for PV_1, PV_2, and PV_3, respectively. By the time t reaches 155.5 ms, the harvested power equals the available power in the PV-arrays. Third, the PV's current also is

affected; they drop immediately following each irradiance. But, they slowly climb up while the external loop regulates the DC-link voltage. As in the available power's waveform, at t = 155.5 ms, each PV current reaches the I_{mpp} with the given light intensity (74.16 A, 51.57 A, 40.27 A).

Table 20: Simulation parameters for the 3PH 7L DC-AC-AC converter.

Parameter	Acronym	Value
Rated Power	P_o	324.16 kW
Output voltage	V_{LL}	13.20 kV
DC-link voltage	V_{DC}	1.00 kV
Switching frequency	f_{sw}	10 kHz
Output levels	m	7
Output frequency	f	50 Hz
Turn ratio	n	4.5
Filter's capacitance	C	9 µF
Filter's inductance	L_i	60 mH
Parasitic resistance of L_i	R_{Li}	100 mΩ
Grid inductance	L_o	129 µH
Grid resistance	R_{Lo}	48 mΩ
Filter's cutoff frequency	f_{cutoff}	6 kHz
DC link capacitance	C_{link}	5000 µF

The test continues in Figure 4.57. Here also, there are three sets of waveforms: (a) The average DC-link voltages, (b) the grid injected currents, and (c) LCL's capacitor voltages. At the beginning of the simulation, a transitory with a peak time equal to 31.25 ms. At t = 0.1 s, the first solar irradiance step is materialized; its effect is seen in (a), (b), and (c) as happened in the previous figure. The set (a) shows the minor perturbation that the averaged DC-link suffers. The inductor current is well controlled, as can be seen in Figure 4.57 (b). There are not considerable overshoots; on the contrary, its shape is purely sinusoidal. In the first interval of time, the RMS value is 14.16 A; during the next period *(t = 1 to t < 2)* the RMS currents drop to 7.29 A, this magnitude is reached after 0.352 ms.

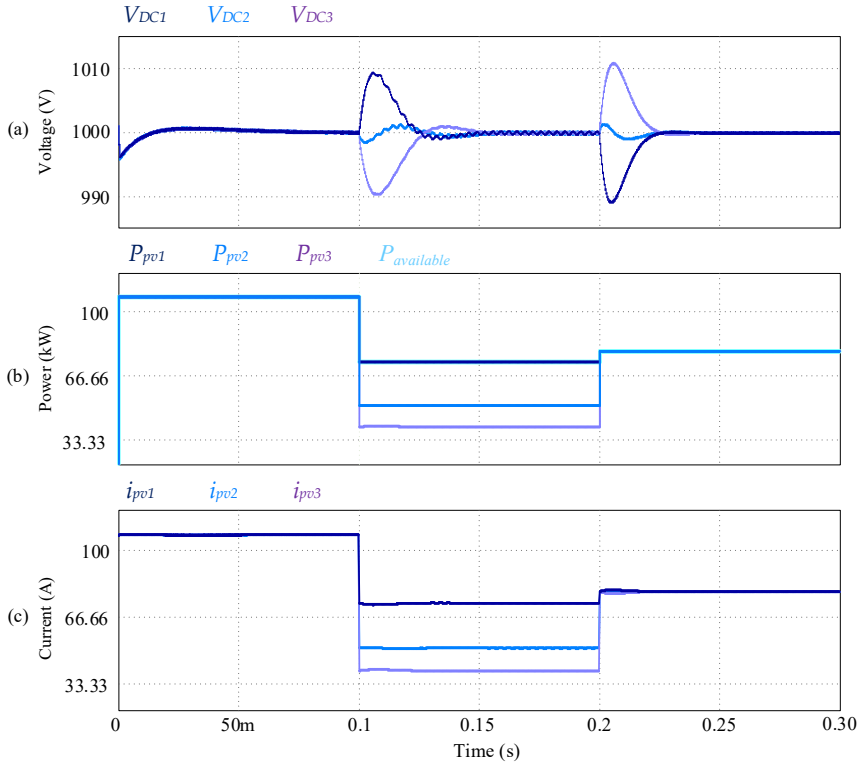


Figure 4.56: Main waveforms of the simulation. (a) DC-link voltages; (b) Available versus generated power in the PV; (c) PV currents.

Finally, in Figure 4.57 (c) is the capacitor's voltage; at t = 0.1 s, there is no deformation of the sinusoidal waveforms, perhaps due to the solar intensity change. Its RMS value remains constant for the entire test (13.20 kV line-to-line). From t = 0.2 s until t < 0.3 s, other transitory shows up in the DC-links. This voltage drift at t = 0.2 s can be practically neglected; at the end of this interval, the voltage settles at 1.0 kV. Regarding the injected current to the grid, its RMS value increases to 10.45 A. Lastly, the capacitor's peak voltage continues stable (18.67 kV) with no alteration all the way to the interval.

The next simulation (Figure 4.58) presents a scenario where one of the PV arrays is not producing any power. The objective of this test is to verify the performance of the controllers and the topology under such critical circumstances. The input parameters of the simulation remain the same, the difference is the irradiance levels in the PV arrays. The irradiance profile is given in

Figure 4.58 (a), the rest of the waveforms are listed as follows. PLL synchronization signal "theta" (b); Grid voltages (c), they are reduced 1000 times so they can be

compared with the inductor's current; modulated signals (d); DC-link voltages (e); Current reference in DQ and measured current in DQ (f).

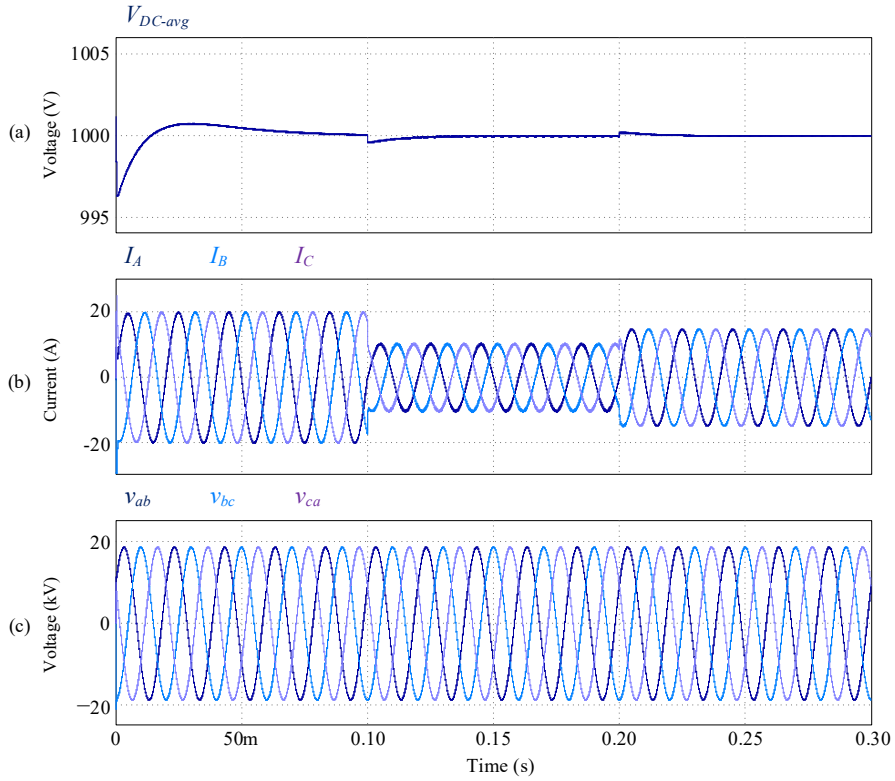


Figure 4.57: Main waveforms for closed-loop simulation. (a) Averaged DC-link voltage; (b) Current injected to the grid, (c) LCL's capacitor voltage.

The first interval of the simulation is $0 \leq t < 0.1$ s. During this period, the irradiance levels are $PV_1 = 1000$ W/m^2, $PV_2 = 1000$ W/m^2, and $PV_3 = 0$ W/m^2. The theta signal is as expected, a ramp that resets once it reaches 2π. The grid voltage is steady without any perturbation, as well as the inductor current, whose RMS value is 7.69 A. The next set of waveforms are the modulated signals that are produced by dividing the three-phase voltage references (v_a, v_b, and v_c) between the three DC-link voltage references (V^*_{DC1}, V^*_{DC2}, *and* V^*_{DC3}), resulting on three sets of modulated signals (v_a, v_b, v_c)/ V^*_{DC1}, (v_a, v_b, v_c)/ V^*_{DC2}, and (v_a, v_b, v_c)/ V^*_{DC3}, that gives nine modulated signals. From those three sets, the one related with PV_3 produce modulated signals of zero amplitude. The DC-link voltages suffer an initial disturbance, but later they are steady with a DC voltage of 1 kV. At the bottom of the section are two signals, the current reference generated by the outer control loop $G_{c2}(s)$, and the inductors current but in DQ frame, so the reference and the measured signals are compared, and it can be verified that the system follows the reference. The next interval of simulation is $0.1 \leq t < 0.2$ s. Here the system suffers from a significant disturbance caused by a

variation in the irradiance levels from two PV arrays changing from 1000 W/m^2 each to 700 W/m^2 and 500 W/m^2, respectively.

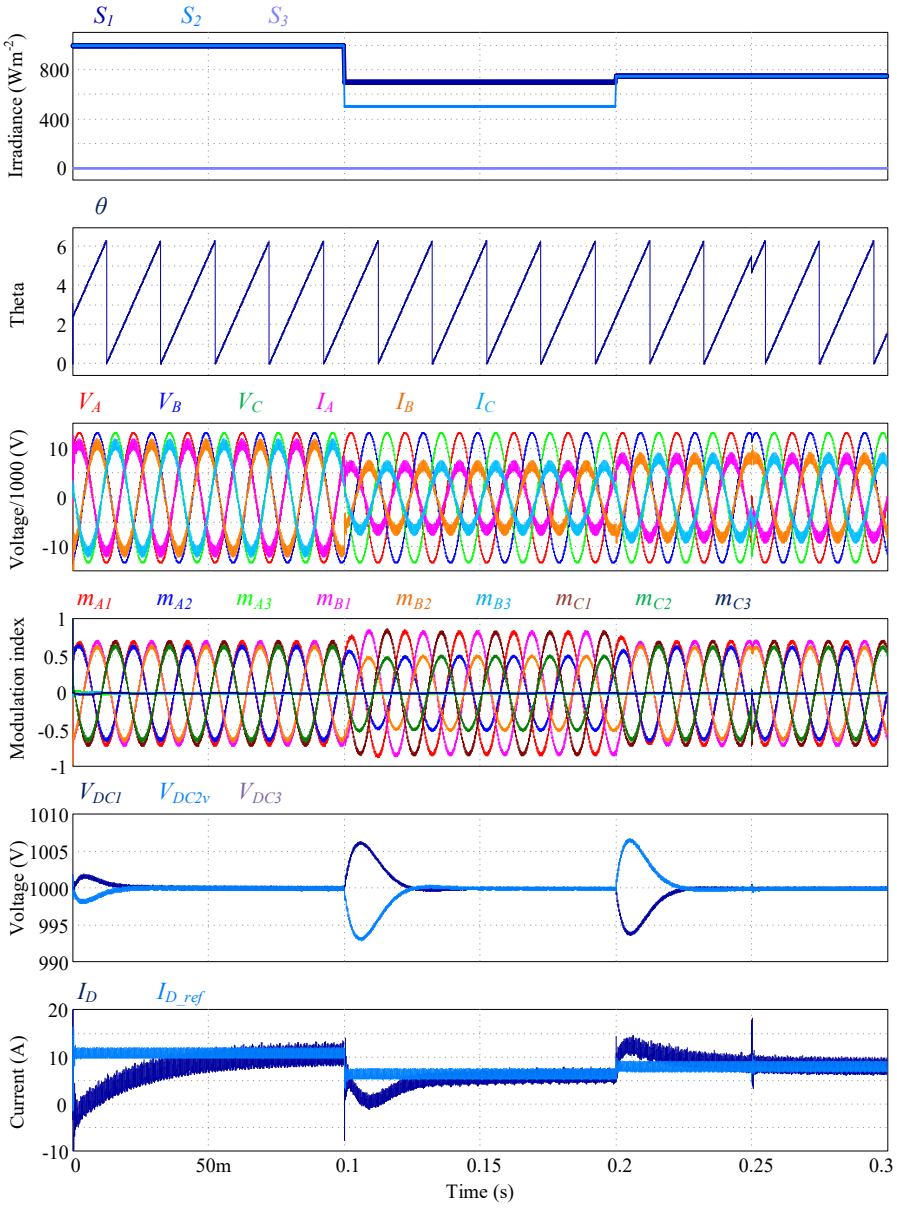


Figure 4.58: Main waveforms for closed-loop simulation. (a) Averaged DC-link voltage; (b) Current injected to the grid, (c) LCL's capacitor voltage.

This produces a drop in the injected current to the grid from an RMS value of 7.69 A to 4.51 A. Another significant change is presented in the modulated signals (d). During the previous period, the modulated signals related to V^*_{DC1} and V^*_{DC2} were the same due to the fact that the power extracted from the respective PV arrays was the same. Now, the three sets of modulated signals are different: m_{A1}, m_{B1}, and m_{C1} are the modulated signals that correspond to the PV array, which produces the most power, and their amplitude are more significant than the rest, while m_{A2}, m_{B2}, and m_{C2} is the set of modulated signals that belongs to the PV array which irradiance level is 500 W/m^2. Then, the PWM signals generated by the larger modulated signal are sent to the top DC-AC-AC cascaded converter. As seen in the waveforms, different modulated signals are generated due to different power processing. Due to the change in the available power in the PV arrays, the DC-links got a perturbation, but this is rapidly controlled (25 ms), and the DC voltages reached the reference again. The last section is the current reference, it is seen that I_{D_ref} changes the reference instantly at $t = 0.1$ s, but the measured signal (I_D) reaches I_{D_ref} again until $t = 0.125$ s.

The last interval is $0.2 \leq t < 0.3$ s. Here the irradiance level on the PV arrays changes to 1000 W/m^2 for PV_1 and PV_2, while PV_3 remains at 0 W/m^2. This change makes the injected RMS current increase to 5.71 A. Now, the modulated signals from the top and the middle cascaded converters reach another operating point with a peak amplitude of 0.71. The DC links are perturbated because of the change in the irradiance, but the steady state voltage is reached quickly at 0.225 s. Finally, the DQ quantities are got as well altered the current reference changes to 8 A at $t = 0.2$ s, and the measured current try to reach this value, but it does not reach it entirely due to at $t = 0.25$ s there is another perturbation.

This new perturbation is a change in the phase of the grid, the 45° phase shift is a sudden and precipitous change that does not represent an actual scenario in a real grid, but this perturbation was triggered to test the PLL and the controllers. As a result, the PLL is able to track the new phase almost instantly, but there are consequences in the system. For example, a peak current (17.60 A) in (f) lasts 1.2 ms; other minor effects can be found in the DC-link voltages. After the last perturbation, the measured DQ current reaches the reference at t = 0.275 s.

As seen in this test, the proposed system can work even when one of the PV arrays is working at zero power. Something to have in consideration is that the modulation index has to be calculated to operate under such circumstances, so the modulated signals do not get in over modulation due to the fact that the system is losing one cascaded converter from $k = 3$ to $k = 2$ in (4.40).

$$m_a = \frac{V_{op}}{knV_{DC}}. \tag{4.40}$$

4.4. GRID-TIED MLI WITH AC-LINK WITH ENERGY STORAGE SYSTEM

In Chapter 3, it was explained how PV and BESS provided by a DC-DC converter could be coupled with the proposed converter. Chapter 4 has proven that the proposed system (Figure 4.6) works properly with an ideal DC-source and with a PV system as the primary input power supply. Therefore, the system under test includes a PV system directly attached to the seven-level, three-phase DC-AC-AC converter. DC-DC converters have not been coupled to the DC side of the three-phase DC-AC-AC cascaded converter so far.

In this section, the entire system is considered (Figure 4.59). The topology is integrated by two stages, DC-DC and DC-AC, with a common DC-link. Two subsystems integrate the first stage, the PV and BESS subsystems which are coupled by DC-DC converters to the DC-link analyzed in chapter 3. The second stage is composed of a three-phase DC-AC-AC cascaded converter studied during the present chapter.

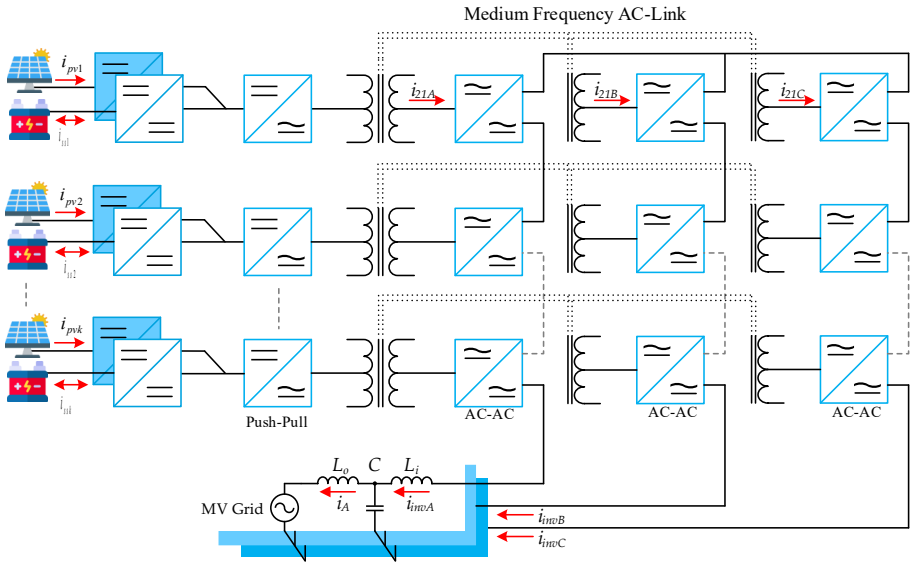


Figure 4.59: A three-phase DC-AC-AC cascaded converter with ESS.

The first subsystem regards the PV modules; these PVs are interconnected in a serial-parallel array to meet the voltage and power level required by the application and regulations. Then, the PV array is interconnected with a three-levels-bidirectional converter (3LBDC) which will extract the maximum power available in the PV array and boost the voltage to a proper DC-link level (1 kV for this simulation).

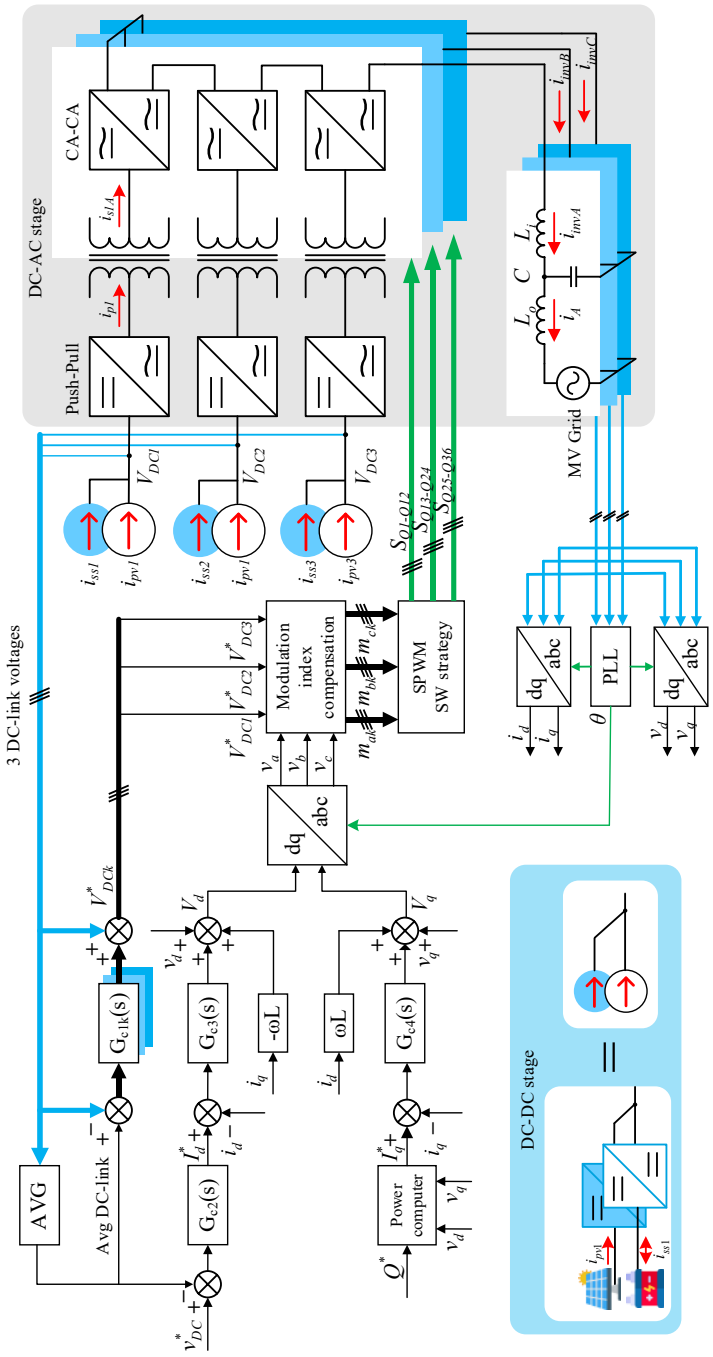


Figure 4.60: Control strategy for the three-phase DC-AC-AC cascaded converter with ESS.

The second subsystem comprises the BESS, which is integrated by a battery array and a 3LBDC converter, which among other things, it will step up the battery voltage (from 250 V) to the DC-link level as well as serve as a charger when the power flows come from the PV or the grid towards the battery. In the second stage (DC-AC), a 3PH 7L DC-AC-AC converter is implemented to interface the PV and BESS subsystems to the utility.

The control strategies are divided into the DC-DC and the DC-AC stage (see Figure 4.60). The DC-DC stage, as explained in chapter 3, includes the PV and the ESS converters (now modeled as current sources for this explanation). Commonly there are two control loops for the PV systems: the MPPT algorithm cascaded with a PI controller (which makes the error from the MPPs tend to zero). In this work, only the MPPT algorithm is taken into consideration. The MPPT directly perturbs the duty cycle in the converter (direct control method) to extract the maximum available power in the PV arrays. Consequently, the system gains simplicity, but due to the lack of a compensator scheme, a small marginal error is allowed. In the case of the BESS, there are two controllers; the first is aimed at controlling the current through the battery while charging or discharging it. The second one aims to control the voltage in the C_{fly} capacitor. If the voltage in this capacitor is regulated at $V_{dc}/2$, then the voltage stress over the 3LBDC switches is reduced by only half of the original value.

The seven-level three-phase DC-AC-AC converter will work in a controlled current source mode feeding the utility. Because the 3LBC converters (PV and BESS) are working in current mode, the DC-link is not controlled yet. As explained in section 4.3.3, there are two main controllers, an external "$G_{c2}(s)$" and an internal loop "$G_{c3}(s)$". In the outer control loop, the average of the three DC-link voltages is regulated to control the output power of the DC-AC stage. During partial shading, a feedforward strategy takes the average voltage of the different DC-links and compensates for the deviations of each DC-link voltage on the modulation index compensation block, as explained in section 4.3.4. Finally, v_a, v_b, and v_c are divided by the signals that the feedforward strategy generated, and the nine modulated signals are obtained.

Then, the modulated signals are sent from the DS 1006 processor to the DS5206 FPGA by the load bus, as explained in section 4.3.6.2. The FPGA will generate the 7 PWM channels that excite the MOSFET's gate drivers, one PWM for the push-pull converter and the other six for the AC-AC converters.

4.4.1. SIMULATIONS RESULTS

The main simulation parameters are available in Table 21. In Figure 4.61, the most representative waveforms of the simulation are drawn as follows: (a) Irradiance level (b) Current in the PV arrays and the BES systems, (c) DC-link voltages, (d) Injected

current to the grid. There are seven intervals through the simulation that aim to test the behavior of the proposed converter under different scenarios.

The first scenario is described as follows. The light intensity for the three PV arrays is 1000 W/m^2 for the time interval, $0 \leq t < 0.1$ s; while the current supplied by the BESS is zero. This is reflected in the voltages' values, powers, and currents; they remain equal in any of the three sets. After the transitory (from 0 to 25 ms), the magnitude of three DC-links voltages is 1 kV. The peak injected current is 10 A; the peak value will be used because it can be read directly from the waveforms so that the reader can follow the explanation of this figure smoothly.

Table 21: Simulation parameters for the MLI with energy storage system of section 4.4.

Parameter	Acronym	Value
Rated Power	P_o	349.50 kW
Output voltage	V_{LL}	13.20 kV
DC-link voltage	V_{DC}	1.00 kV
Switching frequency DC-AC stage	f_{sw_AC}	10 kHz
Switching frequency DC-DC stage	f_{sw_DC}	20 kHz
Output levels	m	7
Output frequency	f	50 Hz
Turn ratio	n	6
Filter's capacitance	C	9 µF
Filter's inductance	L_i	60 mH
Parasitic resistance of L_i	R_{Li}	100 mΩ
Grid inductance	L_o	129 µH
Grid resistance	R_{Lo}	48 mΩ
Filter's cutoff frequency	f_{cutoff}	6 kHz
DC link capacitance	C_{link}	5000 µF
Battery nominal voltage	V_{bat}	250 V
Battery current	I_{bat}	250 A
PV array (mppt) voltage	V_{mppt}	508.33 V
PV array (mppt) current	I_{mppt}	107.51 A

The next period is from $0.1 \leq t < 0.2$ s; here, the irradiance has not been changed, but the BESS is activated at $t = 0.1$; therefore, there is a perturbation on the DC-link

voltages. The perturbation last 30 ms; after that, the DC-link voltages get regulated to 1 kV. The BESS attached to each of the three DC-links injects a different amount of current, which makes the perturbation to the system stiffer; therefore, the controllers, especially those related to controlling the DC-link, have to withstand such perturbation. The current delivery for each BESS (i_{bat1}, i_{bat2}, and i_{bat3}) are 159.92 A, 139.90 A, and 119.90 A, respectively. Then, the injected peak current to the grid increases from 10 A to 16.5 A

The next interval considers from $0.2 \leq t < 0.4$ s. At $t = 0.2$, the irradiance in the three PV arrays changes from 1000 W/m^2 to 650 W/m^2, 450 W/m^2, and 250 W/m^2, respectively, while the injected current on the BESS does not suffer any change. Due to the irradiance change, every array injects a different power (34.28 kW, 23.19 kW, and 12.41 kW each), making the perturbation complex from the controller's point of view. Due to the reduction of irradiance level on the PV arrays, the injected current falls to 10.64 A peak.

The fourth case takes place between $t = 0.4$ and $t = 0.6$ s. For this scenario, the BESS changes from discharging mode to charging mode. For this reason, the current is negative on the three battery banks. Each BESS is charged with 250 A, 225 A, and 200 A, respectively. The available power on the three PV-arrays has not changed, and it is less than the required power for charging the BESS. Therefore, the system stops injecting current to the grid, and at $t = 0.4$ s, there is a current inversion (see the gray area in Figure 4.61, a zoomed view is available on the same waveforms); now, the grid is injecting 6.33 A peak to the BESS. During the transitory, there is a current overshoot of 45%; the transitory lasts 4 ms. This is a strong perturbation that the DC-link voltage controllers expect from the controller point of view; hence, the overshoot is larger with respect to the previous and last 500 ms.

The following stage is $0.6 \leq t < 0.8$ s. The charging currents remain the same, but the PV current increases to 106.47 A, 85.18 A and 63.83 A due to an increment in the irradiance levels on the PV arrays (1000 W/m^2, 800 W/m^2, and 600 W/m^2, respectively). Consequently, the current that the grid is supplying to the battery banks drops to 2.6 A peak. This change in the irradiance alters the DC-link voltage, which produces a transitory that last more than 150 ms.

At $t = 0.8$ s, the BESS switch from charging mode to discharging mode (each battery bank is discharged at a rated current of 160 A, 140 A, and 120 A, respectively); this generates an overshoot on the DC-link voltages, which in the case of the V_{DC2} reach 100 V. The overshot takes 50 ms to disappear. As a result, the BESS is now on discharge mode; therefore, there is once again a current inversion; in consequence, the proposed system injects current into the grid. There is no overshoot, and the steady-state injected current is 14.53 A peak per phase. The PV arrays' irradiance remains the same as in the previous stage.

The last perturbation for this simulation takes place at t = 1.0 s. Here, the battery changes to charging mode again, the difference in this operating point is that the battery is being charged from the available power in the PV arrays and not from the grid as in the previous case. In other words, there is enough power in the PV arrays that they can inject power into the battery and into the grid at the same time. The new battery current references for each battery system are $i_{ss1} = -25$ A, $i_{ss2} = -50$ A, and $i_{ss1} = -75$ A; where the minus sign means that the current enters the battery. Due to the change in the battery operation mode, there are perturbations to the DC-links; the highest peak is 13 V related to V_{DC3}. Additionally, there is a drop in the injected current to the grid, from 14.53 A to 5.8 A, due to some of the power is redirected to the three BESS.

The simulation continues the Figure 4.62; this figure is divided into five sections: (a) Theta angle: this signal is a ramp that resets every 2π, and it is synchronized with the grid voltage. This signal is generated by the PLL block. (b) modulated signals: nine modulated waveforms are grouped in three sets, and every set is related to one of the three cascaded converters. Every set is integrated by three waveforms, one waveform per phase. When the three converters are processing the same amount of power ($0 \leq t < 0.1$ s), it looks like there are only three waveforms, but the others are there with the same amplitude and phase. From $t > 0.1$ s, it is clear that there are nine waveforms, the process of generating them was already explained in the previous figure. (c) DQ current reference and measurement: the reference signal is generated by the outer control loop, and the measurement signal is the current in DQ frame. Here it is evident how the system follows the reference, and it is more evident when the MLI converter injects or absorbs power from the grid. (d) MPPT duty cycles: there are three PV arrays, and consequently, there are three MPPT algorithms. The three signals are the output of every MPPT algorithm, and the output of the algorithm is the reference value that will be compared with the carrier waveform. The perturbation frequency is 750 Hz, and the perturbation step size is 0.002. (e) control signals for the battery controllers: as explained in section 3.4, every BESS has two controllers, one for the charging process and the other for the discharging process. When one controller is operating, the other is kept on hold; if there is a switch in the BESS operating mode, then the opposite applies. For example, in the interval $0 \leq t < 0.1$ s, the BESS is deactivated, then the output of all the controllers is zero. From $0.1 \leq t < 0.4$ s, the discharging mode is active, then the output of these controllers is activated, and in this case, the amplitude is 0.77, while the output of the discharging controllers is kept at zero. Later, during the period $0.4 \leq t < 0.8$ s, the BESS enters in charging mode, then the output of the controllers increases from zero to 0.26, while the output of the discharging controller is kept on hold at 0.77. To conclude, see the interval $0.8 \leq t < 1.0$ s, here, the system returns to discharge mode; in consequence, the discharging controller's outputs are activated again while the controllers for the charging mode are put on hold, and this process continues as required.

As analyzed in this section, all the perturbations that were performed did not make the system unstable; but a formal stability analysis is suggested for future work.

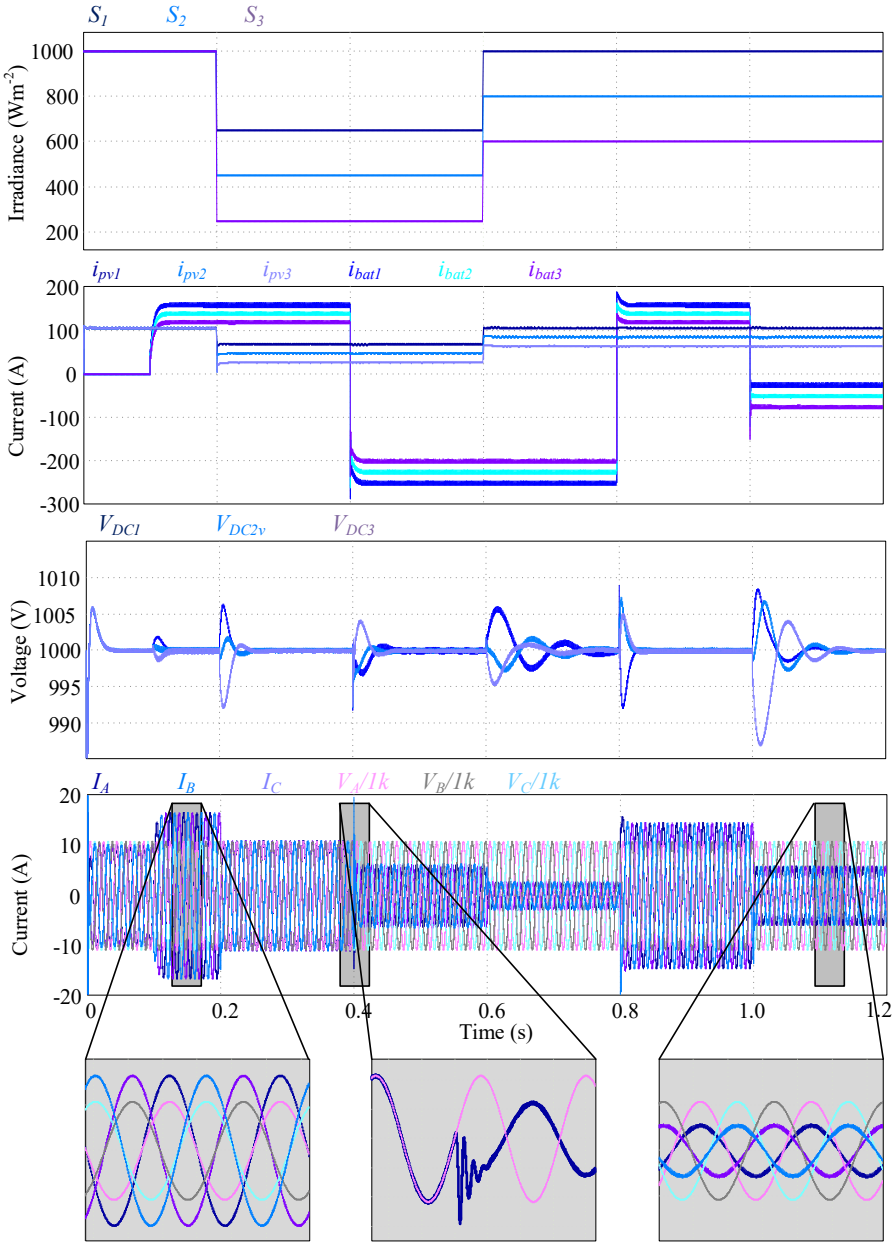


Figure 4.61: Main waveforms of the simulation with PV plus Storage. (a) PV-arrays and BESS current waveforms; (b) DC-link voltages; (c) Injected current to the grid.

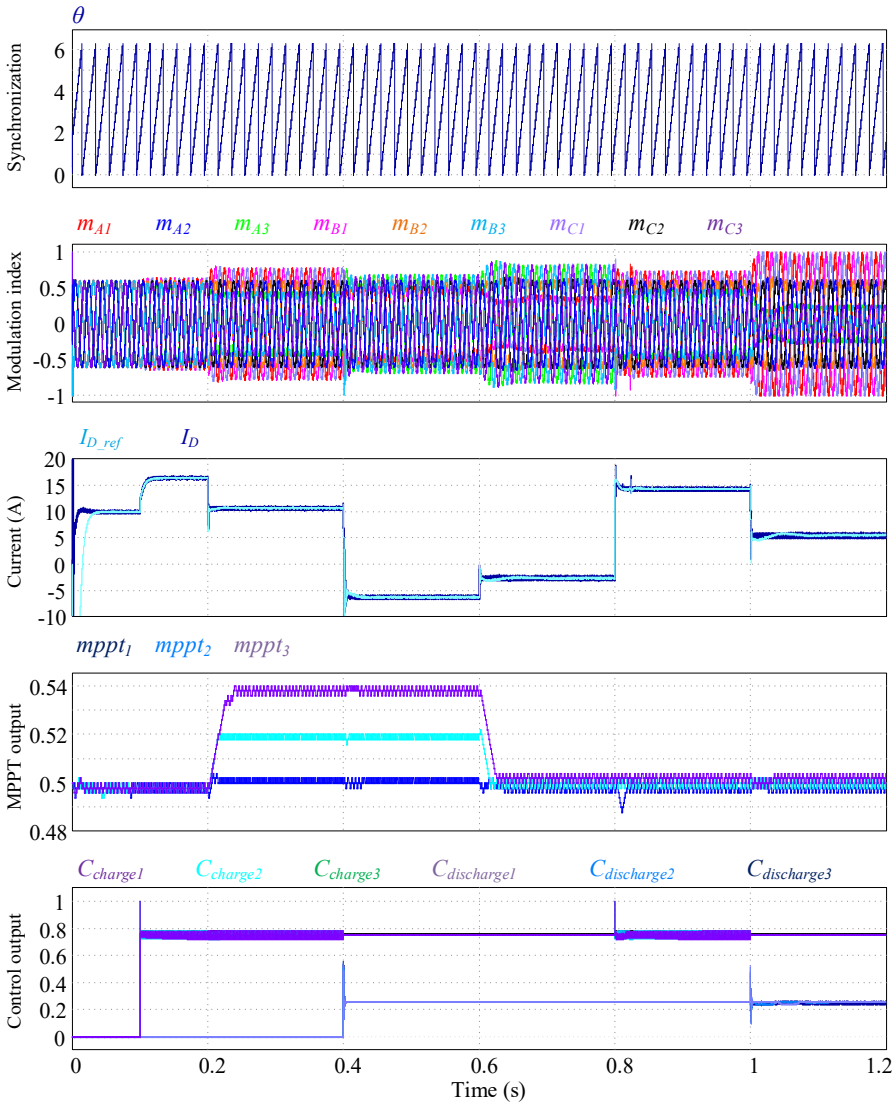


Figure 4.62: Secondary waveforms of the simulation with PV plus Storage. (a) PV-arrays and BESS current waveforms; (b) DC-link voltages; (c) Injected current to the grid.

During the perturbations, the DC-link suffered an overshoot, but its final value reached the reference after a settling time. The three BESS worked in charging mode as in discharging mode, and in general, the proposed converter was able to inject and absorb power towards and from the grid. This series of tests have proven that the three-phase, seven-level DC-AC-AC converter with PV + Battery can work with partial shading and with bidirectional power flow as proposed in this work.

CHAPTER 5. CONCLUSIONS

Humankind is increasing the effort into making the green energy transition possible by generating energy regulations whose aim is to facilitate large-scale renewable energy resources penetration and prevent global warming. Renewable energies are a crucial factor in the decarbonization of the systems. As seen in the introduction, a large number of solar energy systems will be installed in the coming years; therefore, there is a need for new converter topologies to incorporate solar energy into the grid, considering energy storage solutions that enable easy integrations and harvesting of PV solar energy. In this regard, this Ph.D. dissertation proposed a topology based on DC-DC + DC-AC multilevel converters to enhance the conventional grid-tied converter topologies to integrate large-scale PV plants to the medium-voltage grid with battery energy storage support.

For the DC-DC stage of this work, the 3L-BDC converter was introduced, showing its capability to operate together with energy storage systems. Using this converter with interleaved switching allowed the inductor current ripple reduction without the need to increase the inductor size. Additionally, the switches blocking voltage decreased proportionally by controlling the flying capacitor voltage with respect to the input voltage value. This feature is important because, on the one hand, the designer can select commercially low-voltage devices with improved characteristics such as, low turn-on resistance, reduced parasitic capacitances, and forward voltage drop, and reduced prices. On the other hand, controlling the flying capacitor voltage allows the design of high-rated converters that otherwise would not be possible with conventional topologies. In this regard, the 3L-BDC converter, alongside the controllers described in chapter 3, performed the battery charging and discharging process successfully, taking advantage of the converter bidirectionality feature; moreover, this converter was able to achieve MPP tracking in the PV systems while keeping the flying capacitor voltage regulated.

For the DC-AC stage of this work, a DC-AC-AC cascaded converter was proposed. This topology allowed a multilevel output that reduced the THD compared with a two-level topology. Due to the multilevel output and the implementation of a step-up multiple-winding medium-frequency transformer, it was possible to use low-rated low-cost voltage switches. Using a medium frequency, AC-link enabled a transformer volume reduction while keeping isolation between the PV plant and the main grid. The proposed converter cascading structure allowed modularity and the generation of multiple DC links, i.e., as many as cascaded converters. This feature facilitates the implementation of different MPP trackers suitable for large-scale PV plants against partial shading. The use of the multiple winding medium-frequency transformer in this configuration avoided the per-phase imbalance, common among cascaded h-bridge topologies caused by partial shading. In contrast, the proposed converter only presented the usual per-level imbalance found in cascaded topologies. To cope with

this problem, a control strategy was implemented to prevent DC-link voltage drifts that otherwise could lead the system toward instability. Overall, the converter and the control laws let a bidirectional power flow between the proposed topology and the main grid. This means that, under a lack of solar irradiance and low battery state-of-charge, the topology turns into charging mode, and the grid supplies the power. On the other hand, when there is enough energy in the BESS and low solar irradiance, the proposed topology keeps the rated power injection into the main grid, avoiding the PV plant disconnection. In order to validate the above, a simulation made on PSIM was proposed. This simulation included several operation points that proved that the controller and the entire system worked as expected.

A scaled-down prototype was built to verify the three-phase DC-AC-AC converter operation in a laboratory environment resembling real operational conditions. The construction of the prototype considered the magnetic design of the multiple-winding medium-frequency transformer, the thermal design, and the power losses calculation. To validate the converter control used in the laboratory prototype, an implementation was performed using the professional real-time simulator Typhoon HIL alongside with the dSPACE system. In the experimental part, the multiple winding MF transformer presented a good performance compared to the single-input single-output version tested in a preliminary version of the DC-AC-AC converter, where the transformer operates without entering saturation mode after iterative designs.

The construction of the laboratory prototype brings some interesting inputs. For a large number of output voltage levels, it will require using many power switches, twenty-two switches for every converter that would be cascaded; additionally, every two switches will require adding power drivers plus their respective DC power supplies. Another interesting challenge is the generation of the PWM signal that every switch's input gate will require; perhaps the controller is not too complex the number of PWM channels and ADC input will be a factor to consider. Fortunately, the PWM signal generation can be done externally to the controller; simple CPLD devices can generate PWM signals. The challenge would be the synchronization of the PWM generators. Moreover, more than one controller could be used because the control signal is slow enough to be sent by serial, ethernet, or USB communication from one controller to another. Additionally, the construction of the MF transformer is an important task; reduced leakage inductance is needed to avoid voltage spikes or voltage ringing on the AC-AC converter attached to the transformers' secondaries if this is not achieved, snubber networks should be needed increasing the power losses.

Finally, the results obtained in this work demonstrated that the proposed converter topology (DC-DC + DC-AC stages) is a feasible alternative to interconnect large-scale PV+BESS to the MV grid. The proposed converter structure made a size reduction possible compared to conventional 2L topologies. The DC-AC-AC converter does not require a rectification stage, leading to a size and price reduction. In the same sense, coupling the battery system in DC avoids the installation of extra

LF transformers and inverters, which would be required in AC coupling, avoiding extra costs. Furthermore, the simulations proved that the proposed topology could operate with bidirectional power flow, charging or discharging the battery energy storage system when required. Lastly, the preliminary hardware test on the scale-down DC-AC-AC converter showed that it is feasible to build a real-scale version of the proposed converter considering all the stages presented in this work.

5.1. CONTRIBUTIONS

This section summarizes the main contributions from the Author's viewpoint:

- A review of PV and battery systems is done, and both systems' mathematical models are developed.
- A power electronic solution to interconnect large-scale PV systems into the medium-voltage grid considering energy storage. The proposed converter presents the following features:
    - A medium-frequency (MF) AC link that isolates the PV plant from the utility while reducing the size of the transformer
    - A multilevel output that enhances the THD
    - Use of low-rate power switches
    - Modularity
- The control structure described in 4.3.4 allows the PV system to work correctly under partial shading circumstances while keeping the multiple DC-link stables. Additionally, this structure was upgraded to work with the proposed converter (Figure 4.59) considering the Battery Energy Storage Systems (BESS) with PV.
- The proposed power converter uses a bidirectional converter to interconnect the BESS with the PV arrays. Here, control structures have been implemented to charge and discharge the battery system appropriately. The PV arrays or the utility can charge BESS as required.
- Controller hardware in the loop simulations and hardware test on the scale-down prototype proved the operation and performance of the power electronic converter as well as the control structures developed in this thesis. The testbeds include all the necessary electronic boards to operate and control the HIL and hardware converters.

5.2. FUTURE WORK

This thesis presented a deep understanding of the proposed power electronic converter; even though, the author considers that the following are examples of research areas that can be further investigated:

- Construction of the 3L bidirectional DC-DC converter; hence the DC stage can be tested; this includes the bi-directionality of the converter, battery

charging and discharging strategies with an actual battery, and the MPPT implementation with a PV array.

- Construction of at least one extra three-phase DC-AC-AC converter so the multilevel configuration can be tested in a laboratory environment. So far, the multilevel structure has been tested only with two single-phase converters.
- Interconnection of the AC stage (three-phase DC-AC-AC converter) to the grid to verify the PLL operation and the grid-connected control strategy under experimental verification.
- Interconnection of the DC and AC stages so the full proposal can be tested under an experimental environment.
- Stability analysis of the plant model considering the proposed controller structure.
- Develop state-of-charge strategies to regulate how to charge or discharge the BESS properly.
- Design a controller strategy to run the complete proposed structure in off-grid mode for microgrid operation, considering whether the PV stage will work in MTTP or voltage control mode. Until now, and through Chapter 4, and appendix 2 it was proven that the DC-AC-AC converter stand-alone or in cascaded mode, can work as a grid forming converter.

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APPENDICES

Appendix A. FPGA model

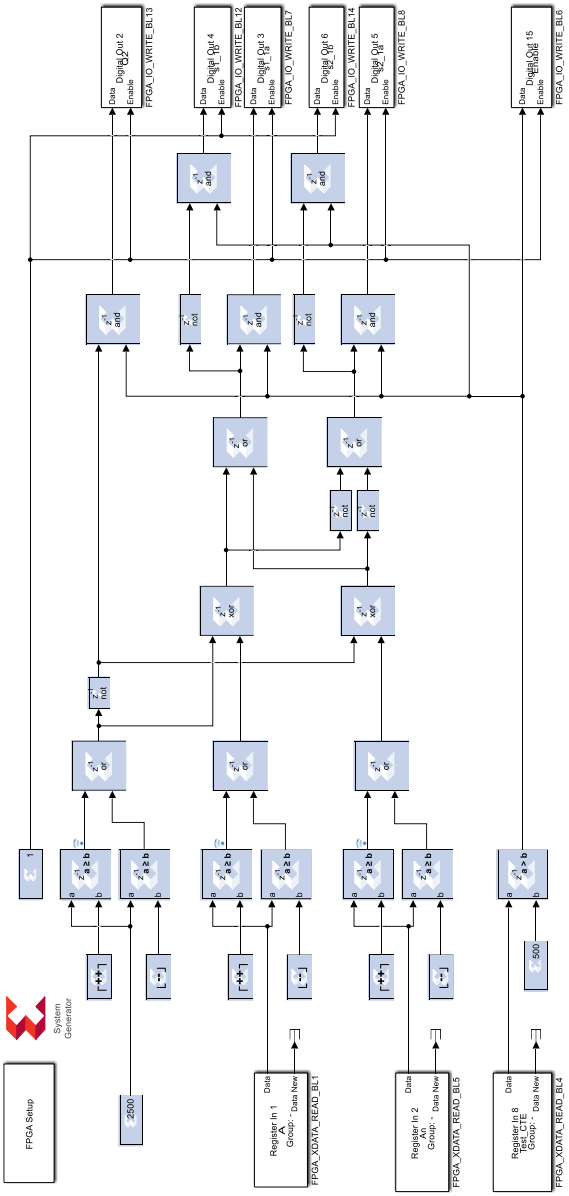

Figure A.1: Inside the FPGA block: PWM generation and switching strategy.

Appendix B. Battery modeling

This mathematical model (Figure A.2) describes the electrochemical battery (Lead-acid, Nickel–metal hydride, Nickel–cadmium, Lithium-ion, among others.) behavior directly in terms of the terminal voltage, open-circuit voltage, internal resistance, discharge current, and SOC; additionally, this model represents the charge and discharge process of the battery [34]. This model only requires the SOC as a state variable to reproduce the datasheet charging and discharging curves. The battery model is implemented using a controlled voltage source in series with a resistance representing the V_{oc} and the internal resistance R of the battery, respectively. The equation (A.1) describes the generic mathematical model based on the work developed by Shepherd.

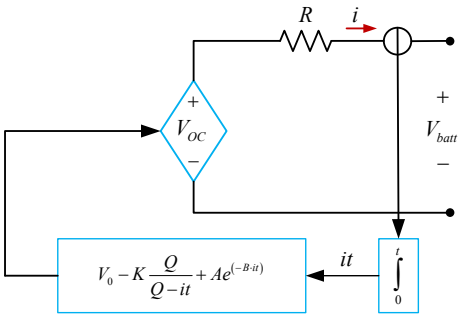

Figure A.2: Sthepherd battery model.

$$V_{oc} = V_0 - K\frac{Q}{Q - it} + Ae^{-B \cdot it} \tag{A.1}$$

Where:

- V_0 is the battery voltage constant [V].
- K is the polarization constant [V/(Ah)].
- Q is battery capacity in [Ah].
- it is the actual battery charge [Ah].
- A is exponential zone amplitude [V].
- B is the exponential zone time constant inverse $[Ah]^{-1}$.
- i is the battery current given in [A].

The SOC is the ratio it/Q. To calculate it is necessary integrate the battery current and consider the initial capacity of the battery:

$$Q_0 + \int_0^t -i\,dt = it \tag{A.2}$$

The Shepherd equation, where the equation (A.1) is based on, has the next nonlinear term

$$K\left(\frac{Q}{Q-it}\right)i \tag{A.3}$$

represent the nonlinear voltage, which changes with respect to the current amplitude and the actual battery charge; therefore, when the battery is fully discharged, and there is no current flow, the battery voltage increases near V_0. As soon as the current starts to flow through the battery, the battery voltage will fall abruptly, describing in this way the actual behavior of a battery under the same circumstances.

This mathematical description makes it possible to represent the behavior of V_{oc}, but creates an algebraic loop and instability problems in simulations. To avoid this challenge [142], the equation (A.1) was implemented, representing a nonlinear voltage, but only depends on the battery's actual charge. In other words, when the battery is fully discharged, and there is no current flow, the battery voltage will be approximately 0 V. Therefore, this model presents results considerably precise while keeping a good representation of the battery behavior. Next are some considerations and limitations regarding the battery model represented by the equation (A.1).

Considerations:

- The internal resistance kept contact in every moment
- The model parameters are obtained from the datasheet discharging curves, and they are considered the same for the battery charging mode
- The battery capacity does not change with the current amplitude (there is no Peukert effect)
- The temperature does not modify the model behavior
- Auto discharge is not considered
- The battery does not have a memory effect

Limitations:

- The minimum voltage without load is 0 V, and there is no limit for the maximum voltage
- The minimum battery capacity is 0 Ah, and there is no limit for the battery capacity; thus, the SOC can be higher than 100 %

This mathematical model represented by the equation (A.1) also called the generic model, can represent various kinds of batteries, depending on the parameters loaded to the model [143]. It is common to find those parameters on the manufacturer's datasheet, specifically in the discharging curves. Figure A.3 shows the discharging

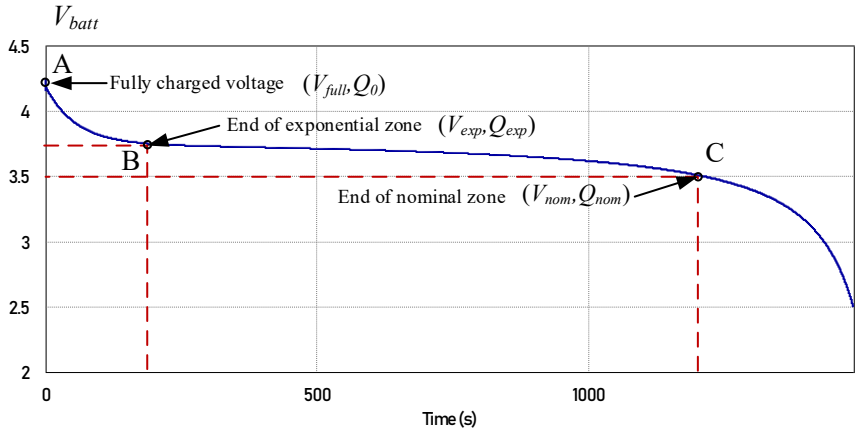

Figure A.3: Discharge curve of a NCR18650GA Panasonic battery.

curve of a Panasonic Lithium-Ion battery (NCR18650GA) composed of Nickel Manganese Cobalt (NMC). The main electrical parameters of the batteries are a nominal voltage of 3.7 V and a capacity of 3500 mAh. The discharging curve is rated at 8 A, which is equivalent to a 2.29 C, where C is the battery's nominal capacity given in Ah.

On the discharge curve (Figure A.3) are three key points required to extract the model parameters: end of the nominal zone (V_{nom} and Q_{nom}), end of exponential zone (V_{exp} and Q_{exp}), and fully charged voltage (V_{full}). The constants A and B from the equation (A.1) are obtained from the points mentioned above as follows:

$$A = V_{full} - V_{exp} = 4.2V - 3.75V = 0.45V \tag{A.4}$$

$$B = \frac{3}{Q_{Exp}} = \frac{3}{0.44A \cdot 1h} = 6.75(Ah)^{-1} \tag{A.5}$$

Regarding the polarization voltage constant K, it is necessary to use the points from the end of the nominal zone as well as the point fully charged voltage:

$$K = \frac{\left(V_{full} - V_{nom} + A \cdot \left(e^{-B \cdot Q_{nom}} - 1\right)\right) \cdot \left(Q - Q_{nom}\right)}{Q_{nom}} = 0.0125V \tag{A.6}$$

Finally, the voltage constant V_0 is obtained from the fully discharged voltage point:

$$V_0 = V_{full} + K + Ri - A = 3.98V \tag{A.7}$$

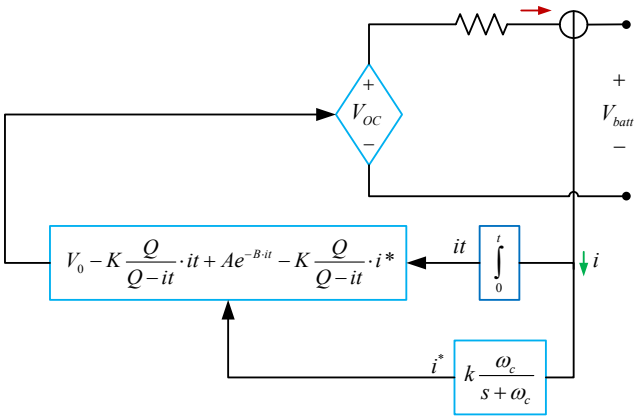

Figure A.4: Battery modified generic model.

The fidelity of the parameters depends on where the three crucial points are taken from the discharge curve.

To summarize, this battery model is an alternative version of Shepherd's model here. This model uses only the battery's SOC as a state variable to represent the battery voltage. The polarization voltage is used instead of the polarization resistance to avoid the algebraic loop and instability problems when it is implemented on simulators. The aforementioned statement is valid only in steady-state, in other words when the battery current is constant, but some erratic behaviors may occur when the battery current is not constant.

A new mathematical model (Figure A.4) based on the Shepherd equation was developed in [35]. Its main advantage is that it can better describe the battery behavior than the model proposed in the equation (A.1). This new model can represent the battery voltage dynamic with better precision when its current is not constant and consider the open-circuit voltage (V_{oc}) as a function of SOC. To do this, a new term (polarization voltage) is added to the equation (A.1) to achieve a better representation of the V_{OC}. Additionally, the polarization term that was modified for the equation (A.1) is again adjusted to accomplish a better performance. The new equation for this battery model is described by

$$V_{OC} = V_0 - K\frac{Q}{Q-it}\cdot it + Ae^{-B\cdot it} - K\frac{Q}{Q-it}\cdot i* \tag{A.8}$$

The last equation's variable definitions are the same as from its counterpart equation (A.1). In addition, there is a new variable i^* called filtered current; this is the current that flows through the polarization resistance. The filtered current solves the algebraic

loop present in the Shepherd equation. Due to the polarization voltage term of the equation (A.8), the V_{OC} changes nonlinearly with the SOC.

There is a difference between the model for discharging and charging mode, and this is due to the behavior of the end of the charge point, where the voltage ramps up quickly when the battery is up to be fully charged ($it \approx 0$). This behavior is represented by the polarization resistance (A.9), which increases immediately as well.

$$PR = K\frac{Q}{it - 0.1Q} \tag{A.9}$$

Therefore, the equation for a Li-ion battery in charge mode is represented by

$$V_{OC} = V_0 - K\frac{Q}{Q - it}\cdot it + Ae^{-B\cdot it} - K\frac{Q}{it - 0.1Q}\cdot i^* \tag{A.10}$$

The considerations on this improved battery model are the same as of equation (A.1) but there are some differences in the limitations:

- The maximum battery voltage is $2V_0$
- The maximum battery capacity is Q
- The maximum battery SOC is 100 %

Appendix C. C-HIL RT simulations

In this appendix some additional C-HIL RT simulations are added. These simulations are included in this section due to the results are preliminary because the plant model that is designed on the Typhoon HIL Centers (THC) is behaving differently from what must be expected. The results are not satisfactory from the point of view of the author because there are some implementation limitations on the Typhoon HIL simulator:

- The switch model that is being used for modeling the bidirectional switch that is part of the bidirectional H-bridge converter that is attached to the transformer's secondary (used to block the MF-AC voltage), is quite limited. Typhoon support explains that so far there is not a bidirectional single or three-phase H-bridge converter in the THC's library. The proposed solution was to build the bidirectional H-bridge with single-pole contactors.
- The components that can be placed in each core is as well limited. The HIL 604 that is used in this thesis works has eight cores and every core has room for up to six contactors, plus three converters (for more details on how the cores are integrated refers to the manufacturer manual.
- To separate a converter that has more than three converters or more than six contactors, a core coupling is needed. Core coupling is a challenging topic, they must be placed strategically following a set of rules dictated by Typhoon.

Therefore, dividing a converter to it fits properly in the device is a challenging task even with the help of Typhoon support. For the implementation of the plant of the Figure A.5, more work must be done.

In the first test (see Figure A.6) a MLI integrated by cascading two three-phase DC-AC-AC converters is tested. For this test, the two cascaded converters are fed by ideal DC-power supplies, and the output of the MLI is connected to a local load. Previous to enable the controllers near at $t = 0$ s, the converter is working in open loop with a given modulation index, the output waveforms (voltage and current) are unbalanced, but this is an incorrect behavior. The output waveform should be perfectly balanced with and small steady state error, due to the parameters of the transformer and all the devices are ideal. This unexpected behavior is due to the plant model is not working properly. After enabling the controllers, the output voltage reaches the reference, and the unbalance situation gets improved. This test proved that the power electronics converter can operate under a MLI configuration; even more, the control structure used for controlling only one three-phase DC-AC-AC converter is kept unaltered to control two cascaded converters. The changes took place in the modulation scheme, where more PWM signals were generated (as explained in section four) to switch the DC-AC-AC converter in cascaded configuration.

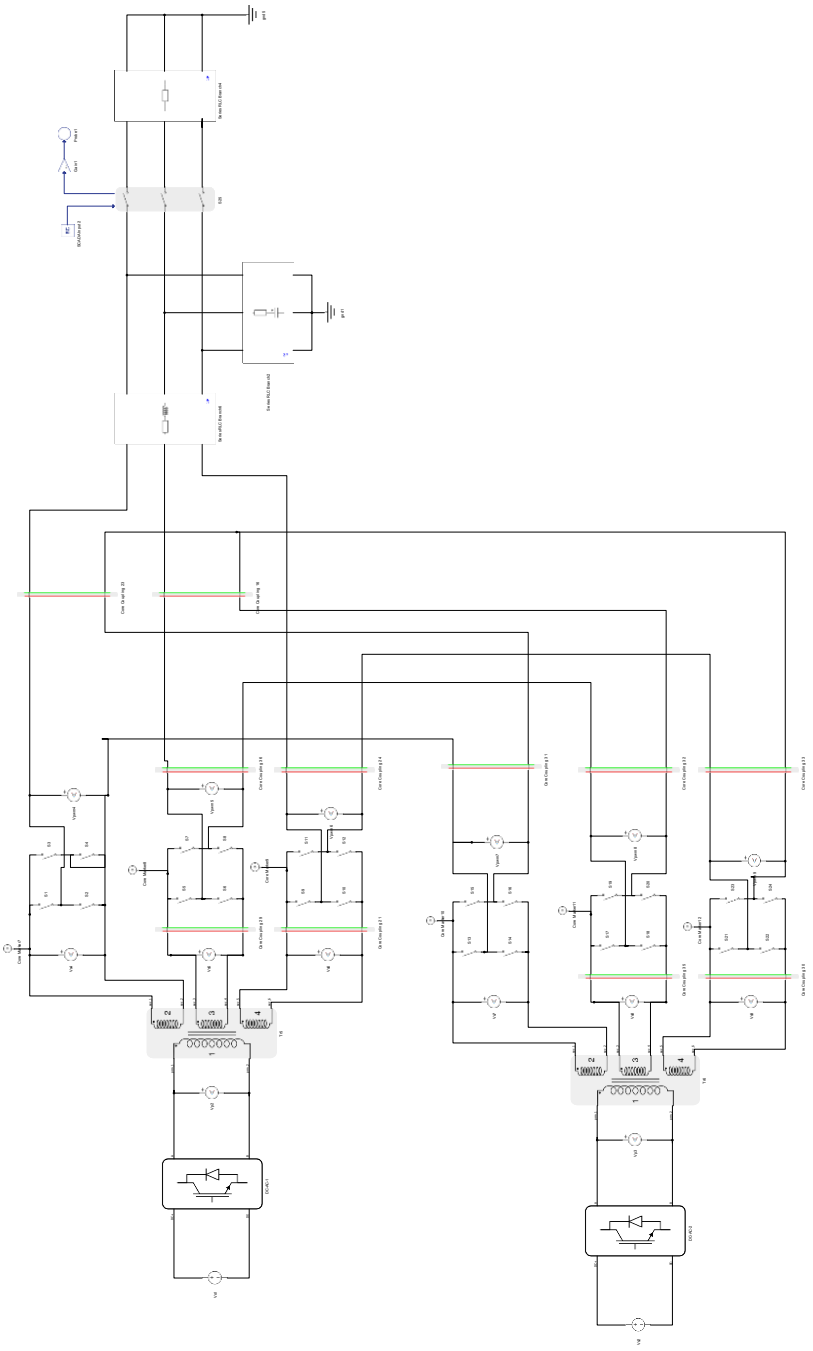

Figure A.5: Typhoon plant model for a 5L DC-AC-AC converter in off grid operation.

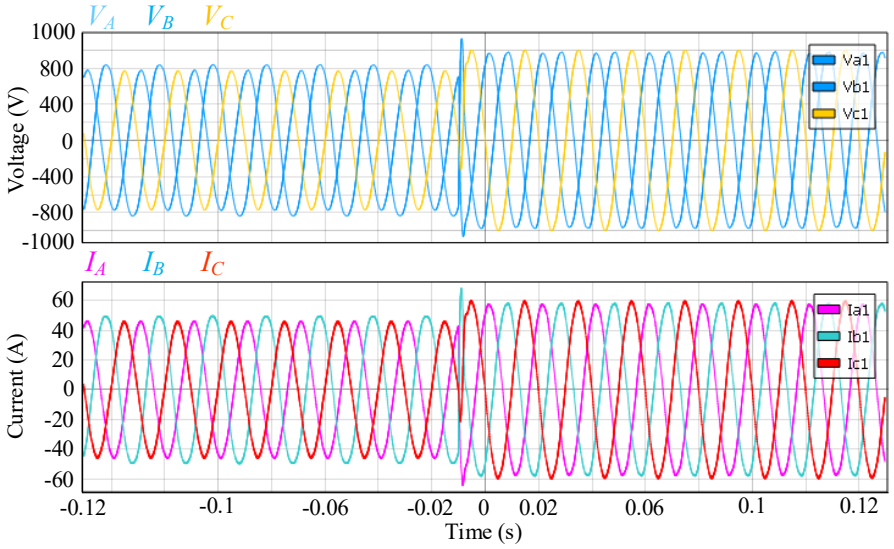

Figure A.6: RT simulation results. (a) Voltage waveform on the load. (b) Load current waveforms.

A final test (Figure A.7) is performed on Typhoon-HIL. This test considers as well as in the previous test, two cascaded three-phase DC-AC-AC, but instead of ideal DC-power supplies as input, a PV array attached to a boost converter is considered to each cascaded converter; additionally, the MLI is feeding the grid.

Every DC-DC converter is performing the MPPT, and the outer control loop is regulated both DC-links as the average. For this test both PV are injecting the same amount of power to the grid. Figure A.8 has three sections: (a) inductor currents; (b) voltage on the PV and the DC-links; and (c) MPPT output. At it is seen the figure, at t = -1.0 s, there is a irradiance step change; therefore the injected current to the grid increases from 13 A peak to 19 A peak. The DC-links got an small perturbation of 6%. The PV-arrays increase its output voltage due to there is more power available on them. And finally, in section (c) it can be seen how the MPPT suffered a change in the generated output which make possible that more power is injected to the grid.

As explained in the beginning of this section, more future work can be done. Firstly, get a more robust power plant that behaves close or equal to the simulations results. Secondly, implement the power imbalance technique to cope with partial shading, because so far in the HIL simulations this has not implemented. And thirdly, add the BESS in parallel to the PV system, so the full system is running on the HIL system. But as mentioned before, the Typhoon HIL 604 that is being used in this work is limited to eight cores, then probably to implement such big plant will require a second device running in parallel with the first HIL.

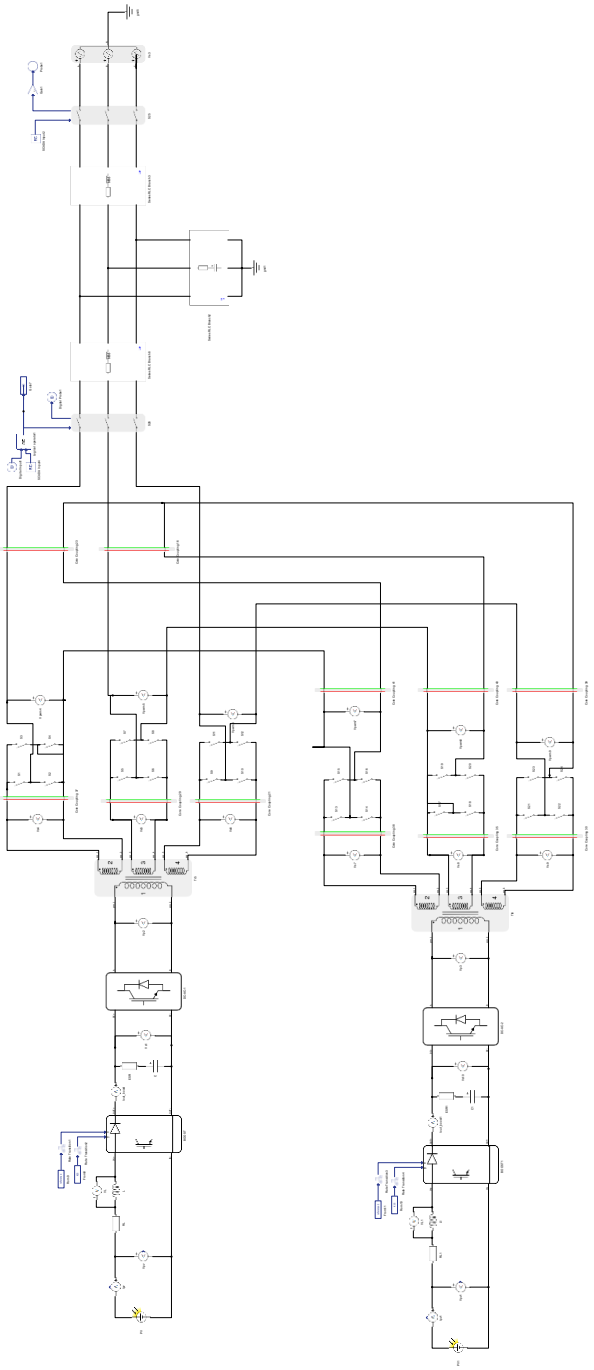

Figure A.7: Typhoon plant model for a 5L DC-AC-AC converter in grid tied operation.

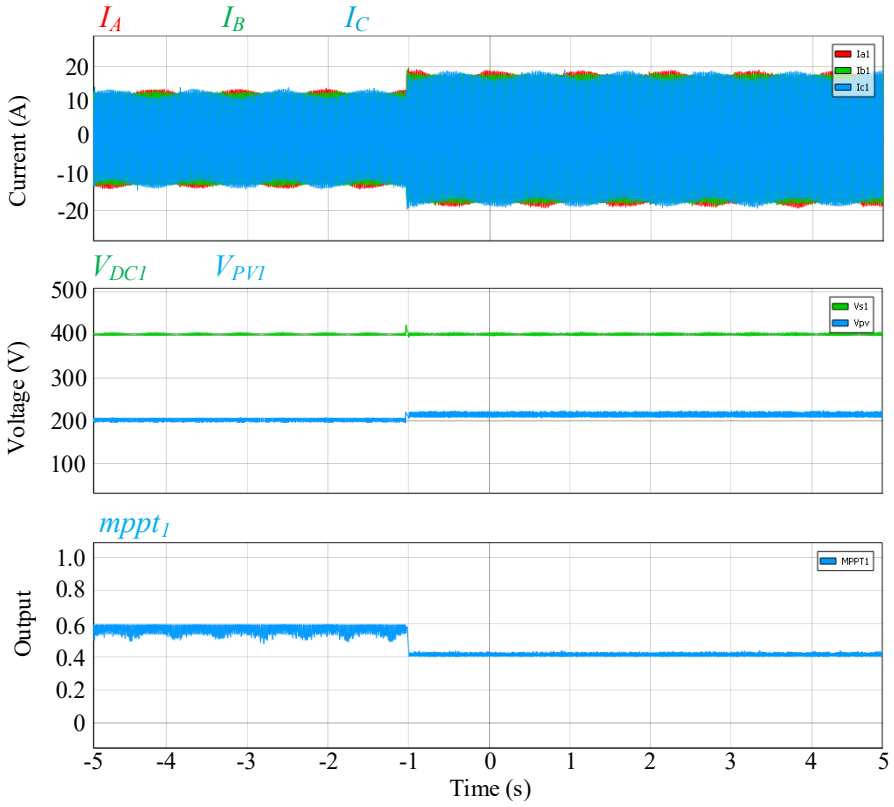

Figure A.8: RT simulation results. (a) Injected current. (b) DC voltages: DC-link and PV. (c) MPPT algorithm output.