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STUDY AND SYNTHESIS OF POWER CONVERTERS FOR ACTIVE POWER DECOUPLING IN LOW VOLTAGE APPLICATIONS

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1. Convertidor Buck – Boost Bidireccional como esquema de desacoplo activo de potencia independiente
2. Convertidor CD/CA con función de desacoplo activo de potencia dependiente
3. Resultados de simulación y experimentales

Conclusiones
Apéndices
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El presente trabajo que lleva por título:

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Se realizó entre Abril de 2021 y Diciembre de 2022 bajo la dirección científica del Dr. Víctor Manuel Cárdenas Galindo.

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Ing. Israel Yepez Lopez

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List of Acronyms and Abbreviations

Acronym	Meaning in english	Meaning in spanish
OECD	Organization for Economic Co-operation and Development.	Organización para la Cooperación y el Desarrollo Económicos.
PV	Photovoltaic system.	Sistema Fotovoltaico.
DC/AC	Direct Current to Alternating Current.	Corriente Directa a Corriente Alterna.
DC/DC	Direct Current to Direct Current.	Corriente Directa a Corriente Directa.
MPP	Maximum Power Point.	Punto Máximo de Potencia.
AC	Alternating Current.	Corriente Alterna.
DC	Direct Current.	Corriente Directa.
APDC	Active Power Decoupling Circuit.	Circuito de Desacoplo Activo de Potencia.
PDC	Power Decoupling Cell.	Celda de Desacoplo de Potencia.
ZVS	Zero Voltage Switching.	Conmutación en Voltaje Cero.
SD	Semiconductor Devices.	Dispositivos Semiconductores.
I/D	Independent/Dependent topologies.	Topologías Independientes/Dependientes.
DSP	Digital Signal Processor.	Procesador Digital de Señales.
DCM	Discontinuous Conduction Mode.	Modo de Conducción Discontinuo.
PWM	Pulse Width Modulation.	Modulación por Ancho de Pulso.
VSC	Voltage Source Converter.	Convertidor en Fuente de Voltaje.
THD	Total Harmonic Distortion.	Distorsión Armónica Total.

Acronym	**Meaning in english**	**Meaning in spanish**
PLL	Phase-Locked Loop.	Lazo de Amarre de Fase.
SPWM	Sinusoidal Pulse Width Modulation.	Modulación por Ancho de Pulso. Senoidal.
SOGI	Second-Order Generalized Integrator.	Integrador de Segundo Orden. Generalizado.
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor.	Transistor de Efecto de Campo Metal-Óxido-Semiconductor.
AWG	American Wire Gauge.	Calibre de Alambre Estadounidense.
IGBT	Insulated Gate Bipolar Transistor.	Transistor Bipolar de Compuerta Aislada.
PCB	Printed Circuit Board.	Placa de Circuito Impreso.
SMD	Surface Mount Technology.	Tecnología de Montaje Superficial.

List of Variables and Symbols

Symbol	Meaning
v_{grid}	Instantaneous electrical grid voltage.
i_{grid}	Instantaneous electrical current.
p_o	Instantaneous electrical grid power.
Z_{grid}	Electrical grid impedance.
v_{pv}	Instantaneous photovoltaic system voltage.
V_{pv}	Average photovoltaic system voltage.
i_{pv}	Instantaneous photovoltaic system current.
I_{pv}	Average photovoltaic system current.
C_{pv}	Photovoltaic system capacitor.
P_{pv}	Photovoltaic system power.
v_{dc}	Instantaneous DC-link voltage.
V_{dc}	Average DC-link voltage.
ΔV_{dc}	DC-link ripple voltage.
i_{dc}	Instantaneous DC-link current.
C_{dc}	DC-link capacitor.
$i_{C_{dc}}$	Instantaneous DC-link capacitor current.
i_o	Output current.
P_{dc}	DC-link power.
ω_0	Electrical grid's angular frequency.
ϕ, θ	Phase angle between the grid voltage and current.
V_p	Electrical grid's peak voltage.
I_p	Electrical grid's peak current.
i_{dp}	Instantaneous current of the active decoupling circuit.
v_{PWM}	Pulsed voltage generated by the power inverter.
L_1	Inverter's side inductor of the LCL filter.
L_2	Grid's side inductor of the LCL filter.
C_f	LCL filter's capacitor.
i_{inv}	Inverter current.
C_z	Decoupling capacitor of the active power decoupling converter.
v_{C_z}	Instantaneous voltage on C_z.
V_{C_z}	Average voltage on C_z.

Symbol	Meaning
L_f	Transfer inductor of the active power decoupling converter.
C_{aux}	Auxiliary capacitor of the active power decoupling converter.
C_1	Split capacitor of the active power decoupling converter.
C_2	Split capacitor of the active power decoupling converter.
v_{C_1}	Instantaneous voltage on C_1.
v_{C_2}	Instantaneous voltage on C_2.
$S_1 - S_6$	Power switches.
$D_1 - D_4$	Power diodes.
η	Global efficiency.
P_{nom}	Nominal power.
I/D	Independent and dependent topologies.
f_{sw}	Switching frequency.
P_{nom}	Rated power.
E_{C_T}	Total energy in the capacitor.
$E_{N_{CT}}$	Total energy in the capacitor (normalized).
E_{C_T}	Total energy in the capacitor.
d	Instantaneous duty cycle.
D_{S_1}	Duty cycle for S_1 of the Bidirectional Buck-Boost converter.
D_{S_2}	Duty cycle for S_2 of the Bidirectional Buck-Boost converter.
L	Transfer inductor of the Bidirectional Buck-Boost converter.
T_s, T	Switching periods of the Bidirectional Buck-Boost converter.
$I_{L_{avg}}$	Transfer inductor's average current.
$I_{L_{max}}$	Maximum peak current across the transfer inductor.
$I_{L_{min}}$	Minimum peak current across the transfer inductor.
f_s	Switching frequency.
I_p	Maximum allowable current across the transfer inductor L.
E_r	Stored energy on the DC-link.
V_{grid}	*rms* electrical grid voltage.
I_{grid}	*rms* electrical current.
r_z	Relationship between the average and the ripple voltage on the decoupling capacitor.
r_{dc}	Relationship between the average and the ripple voltage on the DC-link capacitor.
$V_{S_{1_{max}}}$	Maximum allowed voltage on the power switches.
$I_{S_{1_{max}}}$	Maximum allowed current on the power switches.
R_{load}	Load resistance.
$V_{dc_{max}}$	Maximum peak DC-link voltage.
$V_{C_{z_{max}}}$	Maximum peak decoupling capacitor current.
P_{in}	Input power.
P_o	Output power.
R_d	Relationship between the DC-link and the decoupling capacitor.

Symbol	Meaning
i_{C_z}	Instantaneous decoupling capacitor current.
d_{S_1}	Instantaneous Duty cycle for S_1 of the Bidirectional Buck-Boost converter.
d_{S_2}	Instantaneous Duty cycle for S_2 of the Bidirectional Buck-Boost converter.
$I^*_{C_z}$	Decoupling capacitor's average current reference.
$V^*_{C_z}$	Decoupling capacitor's average voltage reference.
i_h	2nd harmonic present on the DC-link current.
i^*_{dp}	Decoupling current reference.
ξ	Damping factor.
h	Harmonic's number for the resonant filter.
$G_{PI}(s)$	Transfer function of the PI controller.
k_p	Proportional constant.
T_i	Integral time.
C_{in}	Input capacitor.
L_b	Transfer inductor for the DC/AC converter with active power decoupling feature.
i_{L_b}	Instantaneous current across L_b.
l_{inv}	Inductor for the LC filter.
i_{in}	Input current/PV system current.
$v_o(t)$	Instantaneous output voltage.
m_{inv}	Modulation waveform for the Half-Bridge stage.
m_b	Modulation waveform for the Boost stage.
V_r	Peak ripple voltage on the DC-link.
p_{dc}	Instantaneous power on the DC-link
E_{dc}	DC-link energy.
f_c	Cut-off frequency [Hertz].
m_f	Frequency index modulation.
ζ	Damping factor.
j	Imaginary unit.
ω_c	Cut-off frequency [radians].
Z_L	Characteristic impedance.
f_1	Fundamental frequency.
$R_{L_{min}}$	Minimum equivalent resistance.
THD_v	Voltage Total Harmonic Distortion.
THD_i	Current Total Harmonic Distortion.
$V_{Q_{max}}$	Maximum allowed voltage on the power switches.
$I_{Q_{max}}$	Maximum allowed current across the power switches.
$I_{L_{max}}$	Máximum current across L_b.
$V_{dc_{avg}}$	Average DC-link voltage.
$V^*_{dc_{avg}}$	Average DC-link voltage reference.

Symbol	Meaning
i^*_{grid}	Instantaneous grid current reference.
$i^*_{grid_{pk}}$	Peak grid current reference.
v_{in}	Input voltage reference.
v^{α}_{grid}	Filtered signal of the electrical grid.
v^{β}_{grid}	Quadrature signal.
$G_{PI_{PLL}}(s)$	Transfer function of the PLL.
$k_{p_{LL}}$	Proportional constant of the PLL's controller.
$T_{i_{LL}}$	Integral time of the PLL's controller.
$H(s)$	Transfer function of the first-order low-pass filter.
$f_{s_{VSC}}$	Switching frequency for the active front-end rectifier.
$f_{s_{APD}}$	Switching frequency for the active power decoupling circuit.
K_f	Waveform coefficient.
K_u	Window utilization factor.
K_j	Temperature constant.
y	Cooling factor for temperature.
K_f	Waveform coefficient.
X	Geometry factor (ferrites) E-I.
B_m	Magnetic flux density.
W_a	Window area.
A_c	Effective cross-section of the core.
A_p	Area product.
J	Current density.
AWG	American Wire Gauge.
N_I	Initial number of winding turns.
N_T	Total number of winding turns.
l_g	Total air gap.
$l_{g_{real}}$	Real air gap.
N_f	Final number of winding turns.
m	Fringing flux factor.
$B_{m_{max}}$	Maximum magnetic flux density.
$V_{GS_{sp}}$	Miller-plateau voltage.
$V_{GS_{th}}$	Gate-source threshold voltage.
t_{ri}	Rise current time.
t_{fv}	Fall voltage time.
t_{fi}	Fall current time.
t_{rv}	Rise voltage time.
$P_{M_{sw}}$	MOSFET switching power losses.
$P_{M_{cond}}$	MOSFET conduction power losses.
P_{M_g}	MOSFET gate power losses.
P_{M_o}	MOSFET output power losses.
$P_{D_{sw}}$	Diode switching losses.

Symbol	Meaning
$P_{D_{cond}}$	Diode conduction losses.
Q_{rr}	Reverse recovery charge.
P_{T_I}	IGBT total power losses.
P_{D_I}	IGBT's reverse recovery diode power losses.
$R_{\theta_{JC}}$	Junction-case thermal resistance.
$R_{\theta_{CS}}$	Case-sink thermal resistance.
$R_{\theta_{SA}}$	Sink-ambient thermal resistance.

Abstract

The growing worldwide demand and production of electrical energy, coupled with the concern about the growing exploitation of natural resources for the conventional production of electrical energy, has led to the need to incorporate alternative energy sources into the electrical system in order to reduce the dependence on fossil fuels. In addition, the increasing modernization of the concept of electrical grids has promoted the development of new energy generation and distribution schemes to cover needs at different levels of consumption. Under the precedent of these new generation schemes, photovoltaic systems have gained great popularity by making the concept of distributed generation a reality, making the micro-generation of local electrical energy possible through the concept of an electrical microgrid. With the incorporation of microgrid schemes, the need to use power electronics converters for the interconnection of these kinds of systems to the electrical grid becomes fundamental, as well as to reduce the effects of intermittent phenomena in photovoltaic systems. However, it is essential that, despite adapting these conversion schemes, it is important to guarantee that all parts of the system operate in the most efficient way possible, minimizing costs and environmental impacts while maximizing reliability, resilience, flexibility, and system stability.

In a photovoltaic generation scheme interconnected to the electrical grid through power electronics converters, energy storage elements such as passive power decoupling schemes based on electrolytic capacitors are typically used to decouple the oscillatory energy present on the DC-link due to the power supply to the electrical grid. However, the use of bulky electrolytic capacitors entails significant drawbacks such as larger volume and cost of the capacitor and a significant reduction in efficiency, lifetime and power density.

In this thesis work, the analysis and synthesis of power electronics converters as active power decoupling schemes are presented as an alternative to passive decoupling schemes based on electrolytic capacitors.

The objective of this thesis work is to offer a clear panorama of the operation principle of these kinds of conversion schemes. In the first instance, an approach to the fundamental principle of the concept of active power decoupling is addressed. Afterward,

an extensive classification of the different types of power electronics converters for active power decoupling applications is presented. Subsequently, an in-depth comparison is approached between the schemes mostly reported, and their performance parameters are evaluated through a quantitative and qualitative comparison with the data obtained from the reported works. Following this comparison, the two resulting schemes with the highest performance rating are selected; these two schemes are studied in depth in subsequent sections.

The two selected converters are studied in detail and the operating principle, considerations and restrictions, as well as operating regions are addressed. Afterward, the sizing of the passive and active elements for certain operating scenarios is addressed. Thereafter, the structure of the model and the control system's operation used for these converters are addressed. Subsequently, some open-loop and closed-loop simulation scenarios of both converters are addressed for certain operating points and under certain perturbations of interest. The objective of this section is to validate the principle of operation of the converters and the sizing methodology for the defined power conditions.

Consequently, an experimental test scenario is addressed with the built prototypes operated in open-loop to validate the operation principle under the defined power levels. In the appendix section, the design and construction methodology of the converter inductors is detailed as well as the power losses analysis and thermal design. Furthermore, the design and construction considerations of the PCBs for the converters addressed in this work, are approached. Finally, in the conclusions section, the final ideas, contributions and future work proposed for this thesis work are presented.

Introduction

Electricity production and consumption have increased considerably over the years and it seems to keep growing strongly. In 2019, world gross electricity production was 1.3% higher than in 2018. Global electricity production has grown each year continuously since 1974. Generation from combustible fuels accounted for 65.3% of global gross electricity production. Likewise, over the years 2018 and 2019 the global electricity generation from renewable energy resources such as wind (+11.8%) and solar (+22.5%) registered robust growth [1]. Provisional data for 2020 show that gross electricity generation fell 2.4% across the OECD (Organization for Economic Co-operation and Development). Compared with 2019, the electricity mix shifted towards renewables, with lower generation from coal (-15.9%) offset in part by higher output from wind (+12.3%) and solar (+20.8%). In 2021 renewable electricity generation rose by almost 7%, a record 522 TWh increase, with wind and solar PV technologies together accounting for almost 90% of this growth. The share of renewables in global electricity generation reached 28.7% in 2021, after modest growth of 0.4 percentage points [2].

In 2019, the world's total electricity final consumption reached 22 848 TWh, up 1.7% from 2018. In 2019, OECD total electricity final consumption was 9 672 TWh, 1.1% lower than in 2018, while final electricity consumption in non-OECD countries was 13 176 TWh, an increase of 3.8% from 2018.

2021 saw the largest ever year-on-year increase in global electricity demand, with increases in both renewable and coal-fired generation since the total renewable electricity generation reached an all-time high in 2021, exceeding 8,000 TWh, 500 TWh more than in 2020. The increase was driven mostly by rising wind and solar PV production, which grew by 270 TWh and 180 TWh, respectively. The share of renewables in global electricity generation reached 28.6%, increasing by 0.4% from 2020 [3].

A large proportion of the growth in OECD electricity consumption since 1974 has taken place in the residential sector, and the commercial and public services sector. The remaining consumption sectors as transport, agriculture, and fishing are relatively small consumers of electricity. However, road transport has recently experienced strong growth as electric vehicles gain market share across OECD countries, in particular in Europe. It is clear that electricity use is dominated by industry, which represents half of the final

electricity consumption.

1. Photovoltaic systems panorama

The constant increase of electricity production and consumption and the CO_2 global emissions [4], brings the concern of finding new alternatives for implementing new and cleaner energy sources. Solar PV has shown important growth over the years and has a strong prospect.

According to [5], since the beginning of 2020, the cost of producing solar PV modules and wind turbines has increased sharply due to rising commodity prices. Despite this, the power capacity in 2021 has had exceptional growth, since almost 290 GW of renewable power were commissioned this year, which is 3% higher than in the 2020s, and solar PV alone accounts for almost 60% of all renewable capacity. As a prospect, the expansion of solar PV capacity in the next five years is expected to be almost the double that of the previous five years.

In Mexico, for the period 2007 - 2017, the capacity of solar PV generation grew at an average annual rate of 43.2 %. In 2017, the potential of PV solar generation tested in Mexico was around 25 GWh, while the possible resource amounts to 6,500,000 GWh. As a prospective scenario, that gross electricity generation with PV solar technologies is expected to grow at a rate of 21.6% from 2018 to 2032, which implies an increase of 18,732 GWh of new generation produced with these technologies [6, 7].

The exceptional growth and the strong prospective of solar PV promote numerous challenges for electrical grid interconnection, such as power management, power quality, failures, and disturbances support, among others. These parameters must hover within a specific and strict range to be able to interconnect the system to the grid [8]. This is when the performance of power electronics systems is critical and substantial; the incorporation of power electronics systems implies several advantages and brings versatility, nevertheless, it must be guaranteed that the whole system must operate as efficiently as possible, minimizing costs and environmental impacts while maximizing system reliability, resilience, flexibility and stability. In photovoltaic systems, some storage elements such as electrolytic capacitors are widely implemented as passive decoupling elements; however, the use of these passive elements implies several drawbacks that undermine the performance parameters stated above. In this thesis work, a power electronics approach for the substitution of passive conventional decoupling schemes is addressed.

2. Photovoltaic systems interconnected to electrical grid

Generally, a typical photovoltaic generation scheme interconnected to the grid is made up of two power conversion stages: the DC/DC and DC/AC stages [9]. The DC/DC converter meets the task of boosting the voltage on the DC-link and supplying the Maximum Power Point (MPP) of the photovoltaic system [10]. The DC/AC converter (inverter) carries out the function of mapping the energy from the storage system and/or the photovoltaic system and supplying it to the grid. A sinusoidal current signal is generated at the inverter output that oscillates at a certain frequency (regularly 50Hz and 60Hz).

An important aim of the power inverter is to decouple the energy in DC provided by the PV or the storage system from the power delivered to the AC grid. This separation is carried out through a process called *power decoupling*. Typically, this decoupling is based on a passive scheme and is undertaken by a DC capacitor called *link capacitor* [11], which filters the low and high-frequency AC components circulating across the DC side of the power inverter and allows the reactive power exchange between the inverter and the electrical grid. This scheme has the advantage of being very simple because it is only necessary to use capacitors for performing the decoupling task. However, it also has numerous disadvantages such as the size and cost of this capacitor (regularly electrolytic), the reliability, and lifespan, among others [12, 13]. In applications with micro-inverters ($P_o \leq 250W$) some proposals have been made for power decoupling in order to reduce the size of the link capacitor, thus being able to use film capacitors, which have higher efficiency, power density, reliability, and a reduced volume [11, 14]. However, in higher-power applications, it is necessary to integrate more suitable solutions.

3. Power decoupling

An integrated photovoltaic generation scheme with AC mains coupling is usually the one shown in Fig. 1. As mentioned above, the DC/AC converter is responsible for mapping the energy from the DC-link and turning it into AC for supplying energy to the AC grid. The output of this converter is processed by a low-pass filter to remove high-frequency switching harmonics from the AC wave and supplying a sinusoidal current at the determined frequency.

The power on the PV when the MPP is reached is constant, however, the grid's current is time-varying. This difference creates a ripple voltage containing nth-order harmonics on

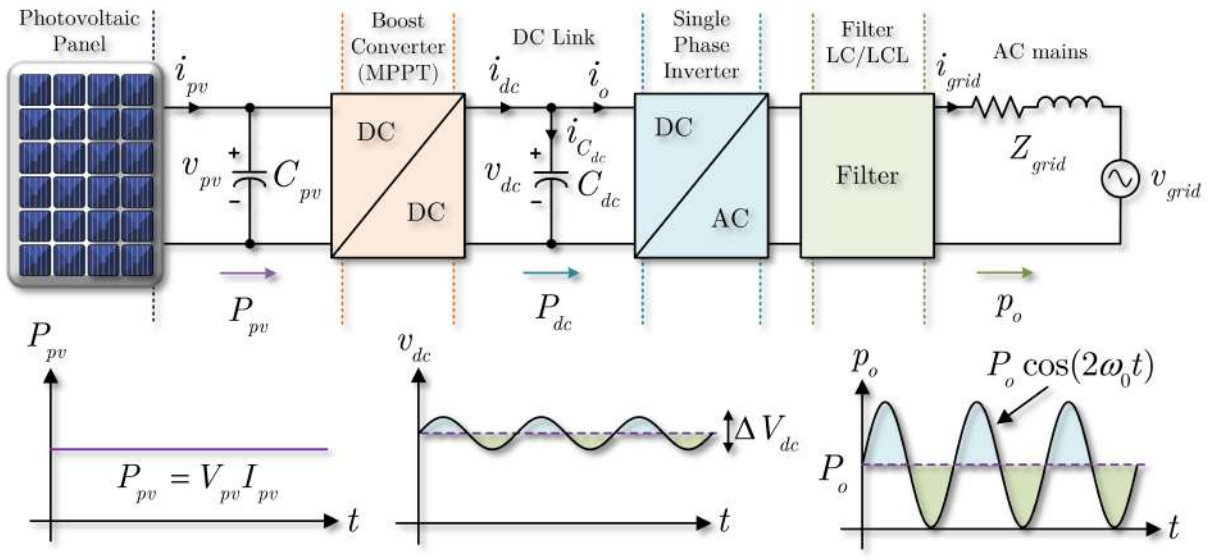


Figure 1. Typical schema of photovoltaic and storage systems interconnected to the electrical grid based on passive power decoupling.

the DC-link voltage. The power on the DC-link is given by the algebraic subtraction of the power at PV terminals (P_{pv}) minus the power supplied to the grid (p_o). When $p_o(t) < p_{pv}(t)$, the overage power is stored by C_{dc}, therefore v_{dc} increases. On the other hand, when $p_o(t) > p_{pv}(t)$, C_{dc} delivers the energy to the grid, consequently v_{dc} decreases. This phenomena causes the ripple oscillation ΔV_{dc} [13]. The power balance arises analytically as follows.

Consider the photovoltaic generation system interconnected to the AC mains through a single-phase inverter represented by Fig. 1. Assuming a lossless operation, the power supplied by the DC-link is given by Eq. 1.

$$\begin{aligned} P_{dc} = P_o &= \frac{1}{T}\int_0^T p_o(t)\,dt = \frac{1}{T}\int_0^T v_{dc}(t) i_{dc}(t)\,dt \\ &= \frac{1}{T}\int_0^T v_{grid}(t) i_{grid}(t)\,dt. \end{aligned} \tag{1}$$

If the voltage and current in the grid are given by $v_{grid} = V_p \cos(\omega_0 t)$ and $i_{grid} = I_p \cos(\omega_0 t - \phi)$, the instantaneous power is given by $p_o(t) = v_{grid} i_{grid}$, that is:

$$p_o(t) = \frac{1}{2}[V_p I_p \cos(\phi) + V_p I_p \cos(2\omega_0 t - \phi)]. \tag{2}$$

Whether the phase angle between the grid voltage and current (v_{grid} and i_{grid}) equals zero, the Eq. 2 can be rewritten as follows:

$$p_o(t) = P_o + P_o \cos(2\omega_0 t) = \frac{V_p I_p}{2}\left[1 + \cos(2\omega_o t)\right]. \tag{3}$$

It can be observed from Eq. 3 that the instantaneous output power is composed of two terms: the average power $P_o = V_p I_p/2$, which is constant, and a second term given by $P_o \cos(2\omega_o t)$ which oscillates at twice the frequency of the grid with an amplitude of the average power supplied at the output of the inverter. The oscillation energy is also present in the DC-link voltage and at the PV terminals. This is critical especially for the PV since its efficiency is reduced and its lifespan is degraded. The simplest solution to this problem is to employ a passive decoupling scheme through energy storage elements (usually DC-link capacitors). The sizing of the link capacitor can be determined by the following expression [13]:

$$C_{dc} \simeq \frac{P_{pv}}{\omega_0 V_{dc} \Delta V_{dc}}. \tag{4}$$

The problem lies mainly in the dimensioning of this capacitor; the passive power decoupling is the simplest of all power decoupling schemas but has the drawback of requiring a very large capacitor, which implies higher costs and volume, while the efficiency of this is diminished by its high series resistance. All these represent a limitation according to the power level that can be managed in this stage and therefore, to the power level that can be supplied to the grid [15]. The proposed solution for this is to perform active power decoupling through power electronics converters replacing passive methods. Fig. 2 shows a structure that represents a basic example of an *Active Power Decoupling Circuit* (APDC) interconnected to a DC/AC conversion scheme. In this case, the APDC is comprised of a DC/DC converter that operates as an active power decoupling scheme; this converter is responsible for buffering the voltage ripple produced by the inverter when mapping the power from the DC-link to the AC mains. The link capacitor is still preserved, however, it can be sized with a much lower value and can be replaced by film capacitors that have lower series resistances, making them ideal for higher power applications. In addition, as the volume of this capacitor is substantially reduced, the cost and efficiency are benefited in the same way.

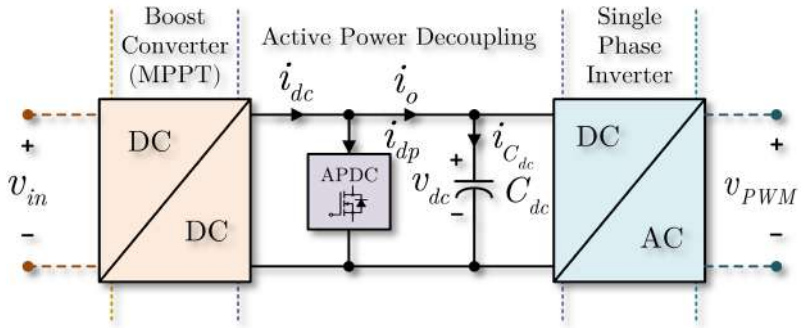


Figure 2. Typical schema of a DC/AC conversion system based on active power decoupling.

4. Active power decoupling

Active power decoupling is a replacement for conventional passive decoupling schemes. The basic principle of an active power decoupling scheme is the same as a passive one; nevertheless, power electronics converters are used to carry out the power decoupling task.

Fig. 3 shows a single-phase inverter with an active power decoupling feature interconnected to the AC mains, and Fig. 4 shows its equivalent electrical circuit. It can be observed from the latter that the APDC is represented by a current source that supplies a compensation current to the DC-link to mitigate the power ripple that oscillates at $2\omega_0$. The operation of this converter can be associated with what is well known as an *active filter* [16]. Depending on the converter topology (series or parallel), it operates as a series or parallels active filter; the difference is that in the first case, it produces voltage drops to compensate for the power ripple, while in parallel topologies the way to attenuate the ripple is through compensation currents [12].

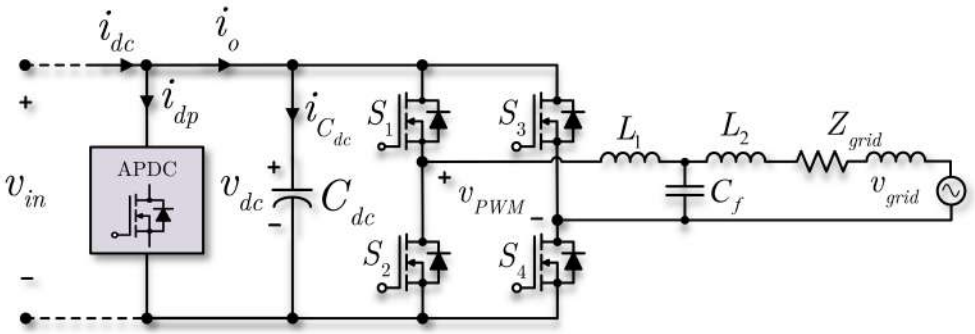


Figure 3. Single phase inverter interconnected to the grid with APDC.

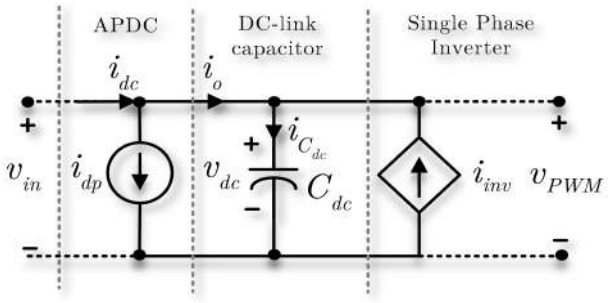


Figure 4. Equivalent electrical circuit for Fig. 3.

5. Active power decoupling schemas

The simplest power decoupling scheme is the passive scheme. As mentioned above, the disadvantages of such schemes are substantial. The most addressed solution in the literature to solve this problem is the implementation of active power decoupling schemes through power electronics converters [17]. Numerous topologies of active decoupling have been reported. Some schemes are more suitable depending on the applications. Nevertheless, it is always desirable to implement low-cost schemes, with the least number of elements and with the greatest reliability and efficiency possible. Fig. 5, shows a classification of the most common topologies for active power decoupling [12]. There are essentially three main categories of active power decoupling schemes: independent and dependent decoupling topologies and the remaining which do not share the characteristics of the above classifications. Independent decoupling structures are power electronics converters schemes that independently meet the decoupling task; that is, these converters have their own active and passive elements to perform the compensation task, and thus, they operate completely apart from the main power converter stage. On the other hand, dependent decoupling schemes perform the same buffering task; however, these partially or fully share the elements of the main power converter stage; this leads to operating the converter in a multiplexed manner, that is, the same elements of the converter can perform two tasks simultaneously through a multiplexing operation.

From the independent and dependent decoupling topologies, a classification for applications in voltage and current sources is derived, using capacitive or inductive energy storage. In this classification, it can be distinguished between series and parallel structures. Parallel schemes regularly use capacity energy storage, while series schemes use the magnetic field properties of inductors to store energy. Although both decoupling series and parallel schemes have individually important advantages, the most used schemes are usually those composed of parallel structures, because from a technological point of view it is much simpler, cheaper, and more efficient to perform capacitive storage. In addition, the use of parallel decoupling schemes allows greater flexibility to develop modulation and control strategies [13].

Independent active decoupling schemes introduce a term known as *Power Decoupling Cell* (PDC). These are commonly formed by modular structures of power electronics converters, which operate independently of the main power converter stage. These same topologies can be extrapolated to dependent decoupling schemes [12, 13, 18]. Fig. 6, shows the most commonly used PDCs for power decoupling applications [13]. Fig. 6-(a), (b), and (c) show respectively the Buck, Boost, and Buck-Boost type cells, and Fig. 6-(d), (e), and

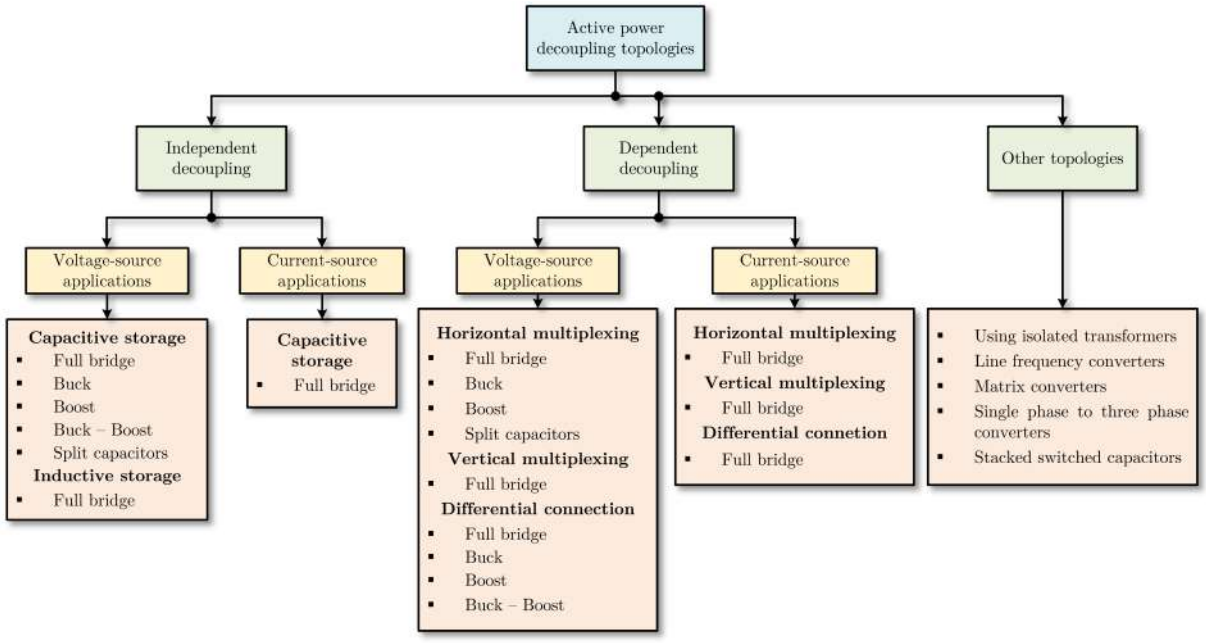


Figure 5. Classification of active power decoupling topologies.

(f) show respectively the basic Full Bridge, Full Bridge with auxiliary capacitor and Full Bridge with split capacitors type cells.

6. Evaluation of active power decoupling topologies reported

From the bibliographic research carried out, it has been possible to identify plenty of topologies used for active power decoupling. However, it was possible to pinpoint that there are indeed a limited number of schemes corresponding to the most frequently found in the literature, which are shown in Fig. 7.

In Fig. 7-(a), the bidirectional Buck-type cell is presented in a grid-interconnected photovoltaic generation scheme. This is one of the most used topologies in the literature for its simplicity, besides that it only requires two switches and two passive elements [13, 18–22]. Fig. 7-(b) illustrates a schema based on a Boost cell. This topology is useful for power ranges above $1kW$ in single-phase applications [9, 18, 23]. Fig. 7-(c) illustrates a topology based on a dependent decoupling scheme based on a half-bridge. In this scheme, the left branch of the full bridge is used to perform the active decoupling task; this topology also features a common mode current rejection function, thus the common mode capacitance is eliminated by connecting the negative terminal of the PV to the neutral of the electrical grid. This represents a great advantage because the use of galvanic isolation

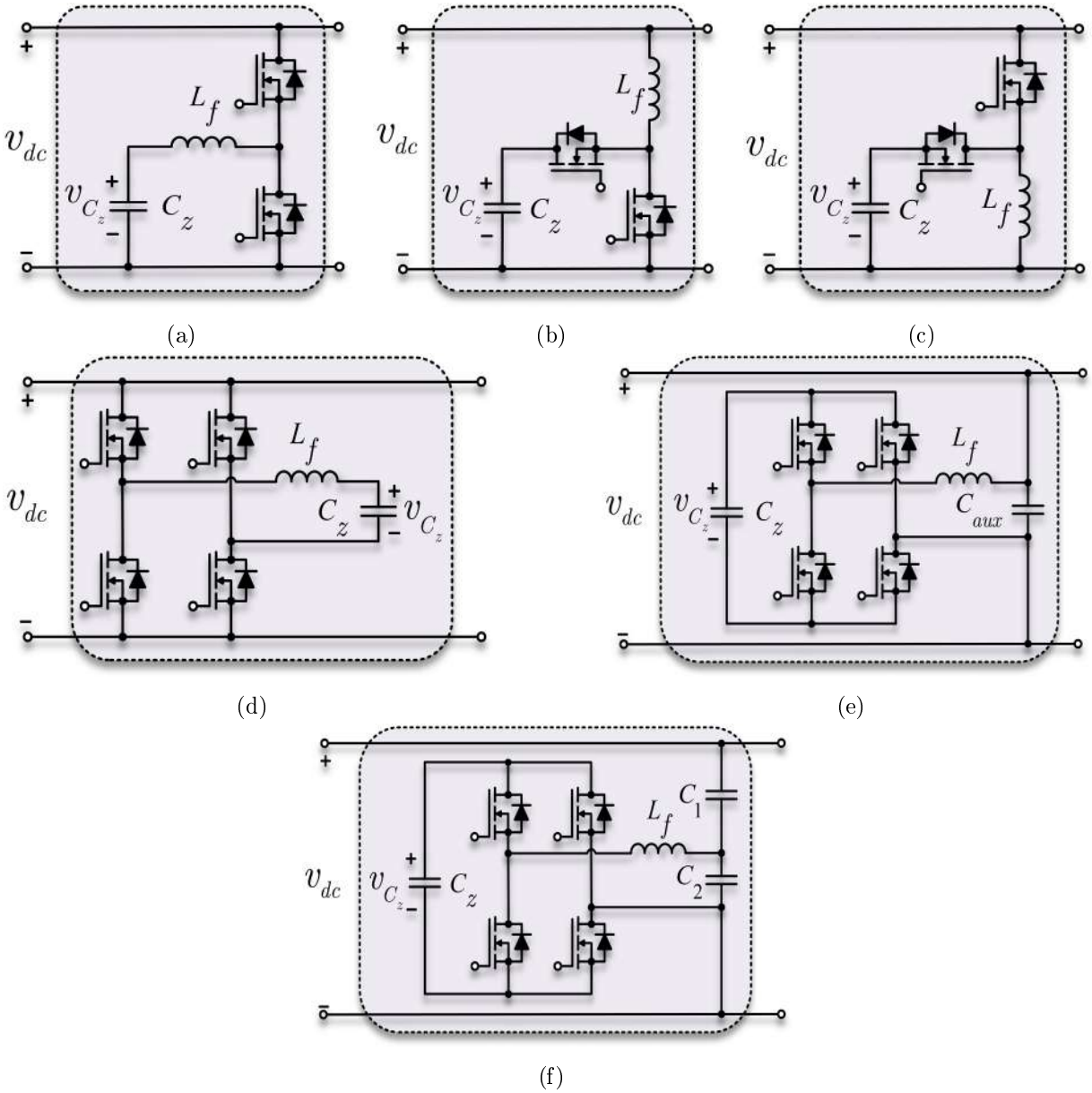


Figure 6. Basic schemes of power decoupling cells. (a) Buck cell. (b) Boost cell. (c) Buck - Boost cell. (d) Full bridge basic cell. (e) Full bridge cell with an auxiliary capacitor. (f) Full bridge cell with split capacitors.

can be avoided in this way; moreover, this scheme reports an overall efficiency of 96.4 % [24–26]. The scheme in Fig. 7-(d) represents a dependent decoupling scheme based on a half bridge; its operation is very similar to the scheme in Fig. 7-(c), nevertheless, two capacitors are used to store the ripple energy and they operate in a complementary way managing half of the energy each half cycle. This topology has mainly focused on reducing current stress on power switches and reaching higher efficiencies since it has been reported efficiencies greater than 93 % [23, 27, 28].

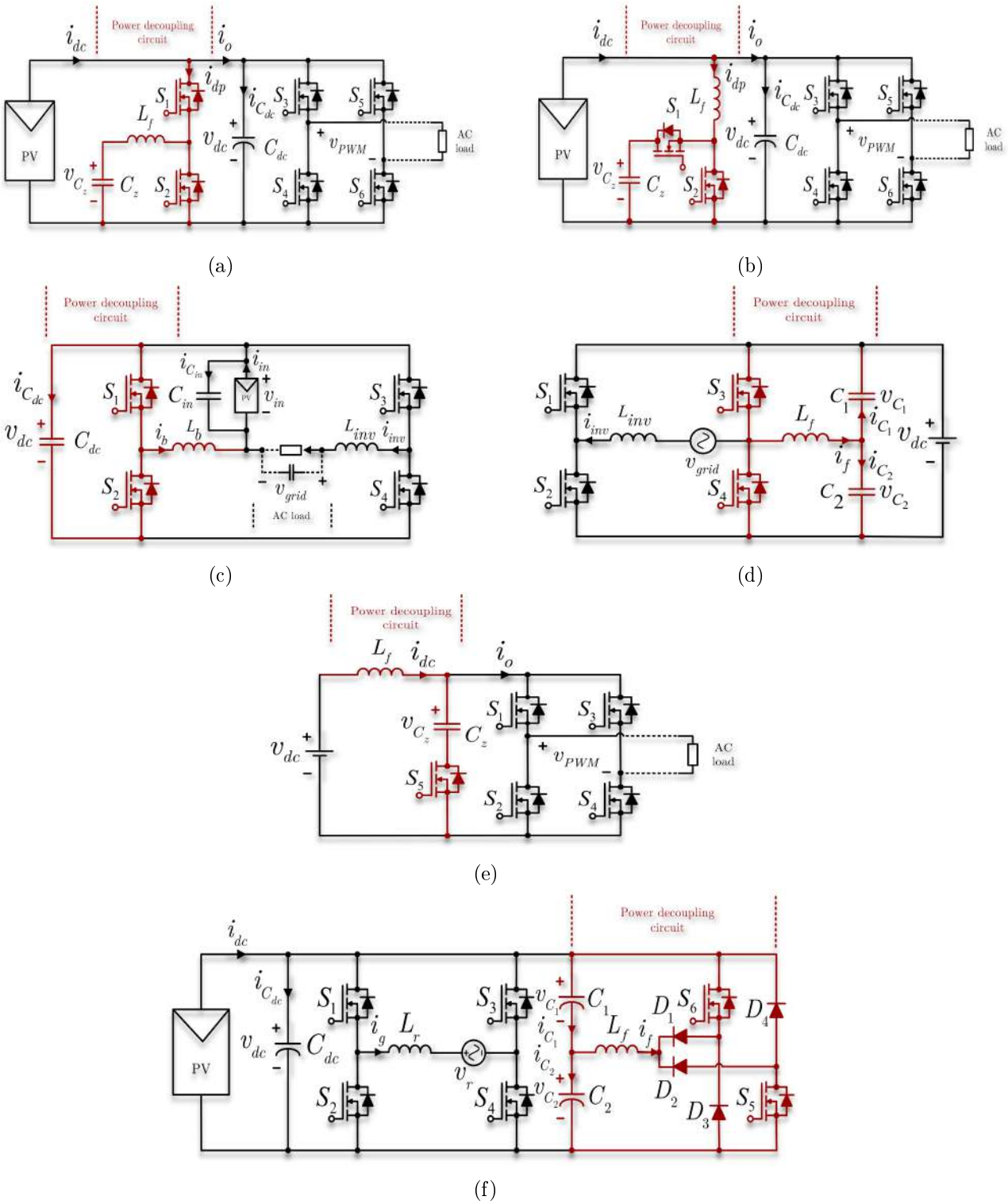


Figure 7. Most common active power decoupling schemes reported in the literature. (a) Buck-type cell. (b) Boost type cell. (c) Dependent decoupling scheme based on a half-bridge. (d) Dependent decoupling scheme with half-bridge and split capacitors. (e) Decoupling scheme with a single switch. (f) Independent decoupling scheme based on a hybrid Dual-Buck converter with split capacitors.

The scheme in Fig. 7-(e) is based on a Boost scheme but stands out mainly for performing the active decoupling task through a single power switch, allowing high-efficiency levels; in addition, by having a single switch, reliability increases [23, 29]. Finally, Fig. 7-(f) represents an independent decoupling method based on a combination between the Dual-Buck converter and the half-bridge using split capacitors as a storage method. Although this topology requires several semiconductor devices, reports efficiencies above 95.6 % [30]. Other reported works use a similar scheme to this that is based on Dual-Buck converters and show good performance at buffering the power ripple [31, 32].

There are some other topologies that do not share the general characteristics of the above topologies. These topologies are based on matrix power converters with galvanic isolated power compensation ports [33–35], however, these schemes report relatively low power densities and use several semiconductor devices. Other topologies also reported are those using float capacitors. The highlights of these topologies are the number of passive elements and the number of sensors, as only two are required. However, the weakness of these schemes is the low power density, the number of semiconductor devices and the efficiency, since at least, four semiconductor devices are required for the power decoupling task [36].

In order to make a comparison and a quantitative and qualitative evaluation of the active power decoupling schemes, the following performance parameters have been defined: schema type, power levels, operating voltages, efficiency, switching frequency, number of passive and active elements, and the normalized energy ($10^{-3}J/W$) that the latter process.

Table 2 shows the most reported topologies for active power decoupling in the literature. All the operating parameters of the reported topologies are grouped in the rows: the type of scheme (series/parallel), efficiency, operating voltages, rated power, switching frequency, values of the passive elements, energy in passive elements, number of sensors, number of semiconductor devices and finally the performance parameters considered for the qualitative comparison. The rating for the qualitative comparison is classified into three colors: green, yellow and red, referring to great, good, and regular performance respectively; this approach is defined by the minimum and maximum performance values found for every topology reviewed. The main objective of this table is to provide a clear idea of which are the topologies with the best performance according to the parameters of interest presented in the Table. 1 and through a qualitative comparison, determine two of the best topologies to carry out its implementation.

Based on the results obtained from the quantitative evaluation of Table 2, three particular topologies can be identified that meet the highest level of evaluation of all performance parameters. The first topology is composed of an active decoupling scheme

Table 1. Performance rating ranges.

Performance parameters	Assessment			
	Regular	Well	Great	Units
Power	$0-1$	$1-2$	>2	kW
Energy in capacitors	≥ 12	$6-12$	≤ 6	$10^{-3}J/W$
Passive elements	>3	3	≤ 2	–
Efficiency	$85-90$	$90-95$	>95	%
Sensors	>4	3	≤ 2	–
Semiconductor devices	>4	$3-4$	≤ 2	–

through the Boost type cell [18]. In this work, efficiencies are reported close to 97% for a rated power of 2kW. Regarding the number of passive elements, this topology uses a film capacitor to store the power ripple and an inductor to transfer it; in addition, only two semiconductor devices are required. The second outstanding decoupling scheme presents a half-bridge based on the bidirectional dependent Boost type topology [24]. In this scheme, efficiencies of 94.6% are reported for a rated power of 3kW. The energy level that passive elements process is very low, as the value of the capacitor is just $2.2\mu F$ with a $400V$ DC-link voltage. In addition, only two semiconductor devices are required to perform the decoupling task. The last outstanding topology corresponds to a schema based on a Buck cell, which has the particularity of operating under a soft switching scheme called *Zero Voltage Switching* (ZVS) [20]. This represents a great advantage because losses in semiconductor devices can be minimized considerably; in this scheme efficiencies of 98.7% are reported. Despite this great advantage, there is a counterpart to the power density that these schemes can process; for this topology, in particular, a power of barely 1kW was reported. On the other hand, this scheme only requires two passive elements and reports positive numbers concerning the amount of energy they process. Only two semiconductor elements are required to perform the decoupling task independently. In the three topologies that stand out, in all cases only two measuring sensors are required: one for the decoupling capacitor voltage and one for the transfer inductor current.

Table 2. Evaluation of most common active power decoupling topologies.

			Converters topologies																			
Parameters		**Units**	[13]	[28]	[31]	[21]	[34]	[35]	[30]	[32]	[20]	[36]	[33]	[25]	[19]	[27]	[18]	[24]	[9]	[23]	[29]	[26]
	Series/parallel	–	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
Fundamentals	η	%	NR	NR	NR	NR	94.4	NR	96.8	96.1	98.7	94.5	97.3	NR	NR	93.9	97	96.4	NR	NR	NR	NR
	v_{grid}	V_{RMS}	220	220	110	120	127	84.85	110	220	220	200	318	220	151	120	240	240	110	110	39	120
	P_{nom}	kW	0.25	1.5	1	3	0.23	0.5	1	2.1	1	1	2.7	1.3	15	1	2	3	0.4	0.4	0.55	2
	I/D	–	I	I	I	I	I	I	I	I	I	I	I	D	I	D	I	D	I	I	D	I
	v_{link}	V_{avg}	420	500	300	250	29.8	200	180	422	400	300	390	450	540	350	400	400	100	200	120	400
	C_{dc}	μF	50	10	110	200	-	44	200	3200		60	50	–	200	–	–	45	–	–	75	50
Converter parameters	f_{sw}	kHz	50	10	NR	NR	30	20	20	40	400	16	NR	2	20	19.2	30	75	12	20	10	100
	C_1	μF	30	155	110	450	38.06	50	80	150	190	180	50	140	140	90	30	2.2	160	50	75	300
	C_2	μF	–	155	110	–	–	–	80	150	–	–	–	140	–	90	–	–	–	–	–	400
	v_{c1}	V_{avg}	250	250	300	250	580	200	180	422	60	300	600	225	520	350	750	350	150	320	120	13.5
	v_{c2}	V_{avg}	–	250	300	–	–	–	180	422	–	–	–	225	–	350	–	–	–	–	–	–
	E_{CT}	J	0.93	9.68	9.9	14.06	6.40	1	2.59	26.7	0.34	8.1	9	7.08	18.92	11.02	8.43	0.13	1.8	2.56	0.54	13.5
	E_{NC1}	$J/W\ 10^{-3}$	3.75	3.22	4.95	4.68	27.83	2	1.29	6.36	0.34	8.1	3.33	2.72	1.26	5.51	4.21	0.04	4.5	6.4	0.00098	6.75
	E_{NC2}	$J/W\ 10^{-3}$	–	3.22	4.95	–	–	–	1.29	6.36	–	–	–	2.72	–	5.51	–	–	–	–	–	–
	E_{NCT}	$J/W\ 10^{-3}$	3.75	6.45	9.9	4.68	27.83	2	2.59	12.72	0.34	8.1	3.33	5.45	1.26	11.02	4.21	0.04	4.5	6.4	0.00098	6.75
	L_1	mH	2	1	1	0.33	0.0001	0.1	2	0.2	0.25	2	0.5	3	0.04	1	1	0.23	0.3	5	10	0.25
	L_2	mH	–	–	1	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Sensors	Voltage	–	1	2	2	1	1	1	2	2	1	1	1	2	1	2	1	1	1	1	1	1
	Current	–	1	1	2	1	1	1	1	1	1	–	1	1	1	1	1	1	1	1	1	1
SD	Diodes	–	–	–	2	–	–	1	4	2	–	–	4	–	–	–	–	–	–	–	1	–
	Transistors	–	2M	2M	2I	2I	4M	5M	2I	2I	2M	4M	2I	2I	2I	2I	2M	2M	2I	1I	2I	2M
Assessment	Power	–																				
	Energy in capacitors	–																				
	Passive elements	–																				
	Efficiency	–																				
	Sensors	–																				
	Semiconductor devices	–																				

NR: Not reported

Regular Well Great

7. Research motivation

The power ripple presented on the DC-link as discussed above is critical. In photovoltaic and energy storage systems interconnected to the single-phase electrical grid, there is always the need of compensating for this power ripple since it can drastically impact and reduce the lifespan of the PV or the energy storage system. Due to the numerous drawbacks of conventional passive decoupling schemes, it is substantial to find and identify emerging ways to provide and contribute to addressing these issues in more suitable manners. According to the background found in the literature, active power decoupling is a topic of paramount interest because of the numerous benefits and advantages it has compared to passive power decoupling.

8. Hypothesis

Based on the issues observed in the approach, the following hypothesis is proposed:
It is possible to encourage, promote and facilitate the development of active decoupling schemes for photovoltaic and energy storage systems as a substitute for passive decoupling schemes through greater transparency, definition, and distinction in the information associated with their concepts, modes of operation, classifications and employing a concrete comparison of two different active power decoupling schemes to provide a deeper perspective and a more intuitive way of selecting these schemes for the various existing applications.

9. Research justification

Nowadays, passive power decoupling is the most commonly used scheme in photovoltaic and energy storage systems. As mentioned above, it has the asset of being the simplest power decoupling scheme, but it also has numerous operating inconveniences. Active power decoupling is novel and a suitable way to compensate for the numerous drawbacks that passive schemes imply. Despite this, active power decoupling seems not to be such a commonly implemented solution for photovoltaic and energy storage systems applications. The wealth of information regarding the active power decoupling issue might provide a blurring panorama of which kind of schemes are more suitable to implement for determining power applications. This thesis work is intended to provide a clearer approach to active power decoupling in order to clarify some issues that may stall its

development and adequacy in the large number of applications where passive power decoupling predominates.

10. Objectives

10.1. Overall objective

Develop an active power decoupling scheme with a reduced-link capacitor integrated into a single-phase inverter interconnected to the electrical grid for active power injection.

10.2. Particular objectives

- Develop an independent active power decoupling scheme based on a power electronics structure without galvanic isolation feature.
- Develop a dependent active power decoupling scheme based on a full bridge converter without galvanic isolation feature.
- Adequate both active power decoupling schemes to a photovoltaic power system interconnected to the grid for active power supply.
- Establish the most suitable control strategy for the system as a whole operating in a photovoltaic system.
- Program control algorithms on a test bench, through their implementation in a Dspace-based control system or a DSP.
- Build both active power decoupling converters and evaluate their performance along with the grid-interconnected power inverter.
- Perform a quantitative and qualitative comparison in order to conclude in which kind of applications these schemes can be used.
- Generate a test bench that allows further developments in the area of power electronics converters for intelligent microgrids.

11. Methodology

In order to accomplish the objectives and scopes raised, the following methodology is proposed:

1. Review of the state of the art of active power decoupling.
2. Perform a quantitative and qualitative comparison of the outstanding active power decoupling topologies in order to select the most suitable schemes.
3. Carry out simulations and experiments to verify the schemes' operation.
4. Develop and validate the schemes proposed through experimental scenarios.
5. Asses the results of the inquiry.
6. Make comparisons between the schemes evaluated and develop conclusions.
7. Report the results obtained through the research.

In the thesis, two different active power decoupling topologies are studied. The first scheme stands for a Bidirectional Buck-Boost converter as an independent active power decoupling scheme which is based on the work reported in [37–39]. The second scheme represents a DC/AC converter with a dependent active power decoupling feature reported in [24]. The overall parameters for both topologies are shown in Table 3.

Table 3. Performance rating for the selected topologies.

Performance parameters	Selected topologies		
	Bidirectional Buck-Boost	DC/AC converter	Units
Rated power	200	500	W
Grid voltage	48	127	V_{rms}
DC-link voltage	100	450	V
Switching frequency	50	50	kHz

12. Thesis scheduling

This thesis work is addressed in three different chapters. Chapter number one introduces the first active power decoupling scheme proposed. First, the operating principle of the power converter is presented. Then passive dimensioning methodology is detailed. Afterward, the converter modeling and the control system are addressed. In chapter two, a second active power decoupling scheme is presented and the same scenarios of scheme number one are also addressed. In Chapter three, some simulations in open and closed-loop are carried out, and then some experimental results in open-loop are given to validate the proper operation of both active power decoupling schemes. Finally, the conclusions of this research are shown, detailing the solutions, contributions, and areas of opportunity in

the different topics covered in this work. In addition, the scientific production during the development of the research work is summarized. Some practical details of the development of this work are explained in the appendices section.

Chapter 1

Bidirectional Buck-Boost converter as an independent active power decoupling scheme

According to the comparative evaluation of the power decoupling topologies reported carried out in the introduction chapter, it has been possible to conclude that there exist three different outstanding power decoupling topologies [9, 20, 24]. This work intends to evaluate the performance of an independent active power decoupling scheme in contrast to a dependent active power decoupling scheme. Of the three outstanding topologies, two of them are independent schemes, but the one which has the highest performance according to the comparative evaluation carried out was taken into account for the implementation. This scheme consists of a bidirectional Buck-type cell. Nevertheless, in some works reported, it has been discussed that this scheme has some restrictions (view Table 1.1), since the voltage in the decoupling capacitor must be lower than the DC-link voltage, and this implies that the decoupling capacitor must have a relatively large value [16, 40]; this phenomenon can be explained by the equation for the energy stored in a capacitor: $E = \frac{1}{2}Cv^2$, where it can be seen that if the capacitor voltage is halved, the capacitance must increase four times to store the same energy on the capacitor. On the other hand, in the Buck-Boost scheme, both capacitance and voltage are adjustable, allowing higher flexibility for dimensioning, selection and implementation. Consequently, the Bidirectional Buck-Boost converter as an active power decoupling scheme has been selected as the independent converter scheme.

1.1. Considerations

Fig. 1.1 shows the Bidirectional Buck-Boost converter. This power converter has numerous advantages of interest: it can operate individually of other conversion stages, then it has a modularity feature; the control system becomes simpler because the power switches meet only a unique task; and finally, as this topology has modularity feature, it can be easily replaced by a passive scheme in order to build comparisons scenarios and evaluate their performance.

Table 1.1. Buck, Boost, and Buck-Boost schemas restrictions.

Parameters	Buck type	Boost type	Buck-Boost type
Decoupling capacitor voltage v_{C_z}	$< v_{dc}$	$> v_{dc}$	adjustable
Decoupling capacitance C_z	relatively large	relatively small	adjustable
Stress voltage	v_{dc}	v_{C_z}	$v_{C_z} + v_{dc}$
Stress current	i_{dc}/d	i_{dc}	i_{dc}/d
Efficiency	-	higher	-

The following considerations must be taken into account for the converter operation (Fig. 1.1) [16, 37]:

1. The decoupling capacitor C_z must bear large voltage ripple oscillations.
2. The transfer inductor L operates in Discontinuous Current Mode (DCM).
3. The stress voltages in power switches are the sum of $v_{dc} + v_{C_z}$.
4. The stress current in power switches is given by i_{dc}/d, where d is the instantaneous duty cycle.
5. Both voltage and capacitance of the decoupling capacitor can be adjustable, but $v_{C_z} > 0$.

1.2. Operation principle

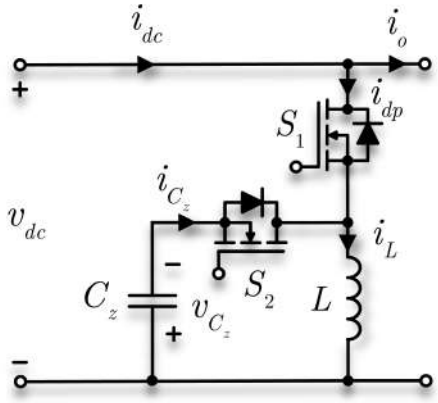
The Bidirectional Buck-Boost converter is a DC/DC power converter that is originally compounded by the basic structure of a unidirectional Buck-Boost converter but two active switches are used to allow bidirectional feature (Fig. 1.1).

The function of this converter is to drive the current's oscillatory harmonic of i_{dc} at $2\omega_0$, through the path of current i_{dp}; that is, they are equal, thus on the current i_o demanded

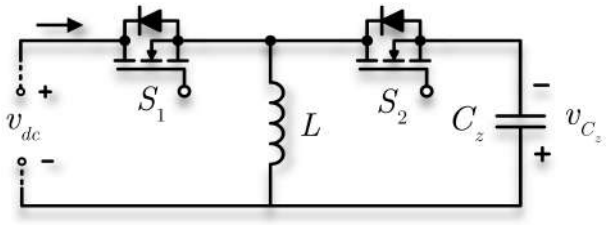
by the load, only the average value is manifested and the ripple energy is stored in the decoupling capacitor C_z. All this can be achieved by allowing a large ripple voltage on this decoupling capacitor; that is, the ripple energy is driven to be stored in C_z instead of C_{dc}, then only the high-frequency components are buffered by C_{dc}, and thus, this capacitance can be substantially reduced. The DC-link and the decoupling capacitor voltages can be related through the duty cycle of the Bidirectional Buck-Boost converter as follows:

$$D = \frac{V_{out}}{V_{in} + V_{out}} = \frac{V_{C_z}}{V_{dc} + V_{C_z}}. \tag{1.1}$$

The Bidirectional Buck-Boost converter has two power switches, S_1 and S_2, and can operate at first in a complementary way. The modulation scheme is very simple; since it is possible to implement a constant PWM. The inductor L meets the task of transferring the power ripple energy from the DC-link to the capacitor C_z.



(a) Bidirectional Buck-Boost converter (view 1).



(b) Bidirectional Buck-Boost converter (view 2).

Figure 1.1. Bidirectional Buck-Boost converter as an active power decoupling scheme.

The Bidirectional Buck-Boost converter operates in two different modes [39]: charge and discharge modes. In charge mode (view 1.2), energy is transferred from the DC-link to the decoupling capacitor through the transfer inductor; while in discharge mode (view 1.3), the decoupling capacitor releases its charge and the inductor transfers it to the DC-link.

These two modes of operation are presented depending on the four possible states of the switches [41]. The first takes place when switch S_1 is on and S_2 off (view 1.2-(a)). At this instant, current flows from the DC-link towards the inductor which stores the energy, and the current tends to grow to a maximum value $I_{L_{max}}$. It is important to remark that v_{dc} and v_{C_z} can be considered constant in each switching period but for larger time intervals, the signals are time variants. Considering then that $v_{dc} \to V_{dc}$ and $v_{C_z} \to V_{C_z}$ in a switching period and the fact that $T_1 + T_2 \leq T$, being $T_1 = D_{S_1} T_s$ and $T_2 = (1 - D_{S_1})\, T_s$, the average current across the inductor during the positive half-cycle can be determined as follows:

$$\begin{aligned} I_{L_{avg}} T_s &= \frac{1}{2} I_{L_{max}} D_{S_1} T_1, \\ I_{L_{max}} &= \frac{V_{dc}}{L} D_{S_1} T_1, \\ I_{L_{avg}} &= \frac{V_{dc}}{2L} D_{S_1}^2 T_1, \end{aligned} \tag{1.2}$$

where T is the whole switching period and T_s the charge mode switching period; that is when the charging mode is completed. It is important to highlight that T_s can be equal to T.

Once this maximum is reached, the second state takes place, where S_1 is off and the free-wheeling diode of S_2 is activated (view 1.2-(b)); in this state, the inductor transfers the energy to the capacitor and this is when the charging mode of the converter is completed. The current's evolution during states one and two is shown in Fig. 1.2-(c).

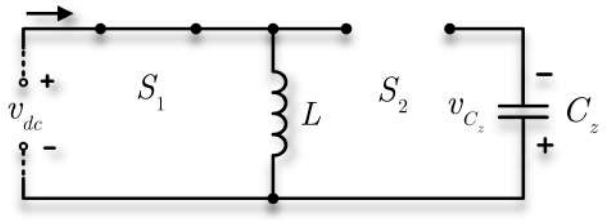
From the Eq. 1.2, the duty cycle for S_1 can be determined as follows:

$$D_{S_1} = \sqrt{\frac{2 I_{L_{avg}} f_s L}{V_{dc}}}, \tag{1.3}$$

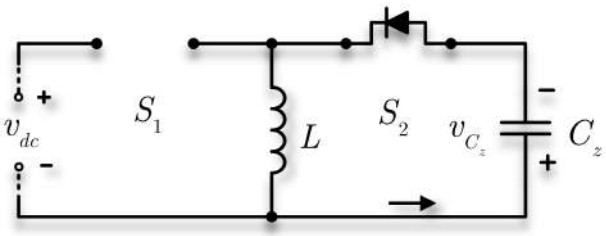
where f_s is the switching frequency of the Bidirectional Buck-Boost converter.

In the third state of the converter, it operates oppositely. In this case, the switch S_2 is on while S_1 is off and the decoupling capacitor C_z transfers the energy to the inductor L (view 1.3-(a)). In the fourth state, switch S_2 is off, and the free-wheeling diode of the switch S_1 is activated, allowing the inductor current to circulate towards the DC-link (view 1.3-(b)); this is where discharging mode of the power converter is completed. The current's evolution during states three and four is shown in Fig. 1.3-(c).

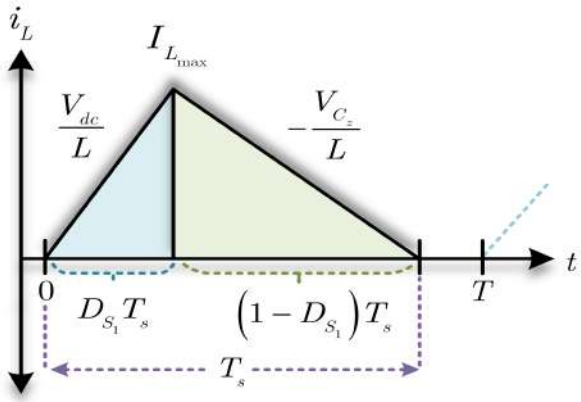
It should be noted that this converter operates in *Discontinuous Conduction Mode* (DCM), since the inductor current is positive in one half-cycle and negative in another. This offers an important advantage, since considering this operation mode and the fact that it is not essential to maintain a low current's ripple, the size of this inductor can be considerably reduced under this criterion and by increasing the switching frequency.



(a) $S_1 \rightarrow ON \rightarrow D_{S_1} T_s$ (first state).

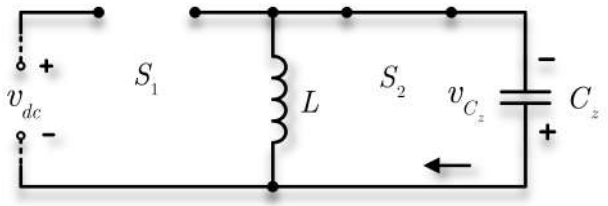


(b) $S_1 \rightarrow OFF \rightarrow (1 - D_{S_1}) T_s$ (second state).

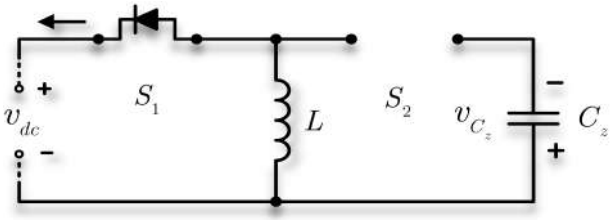


(c) Current's evolution across the inductor during the first and second state.

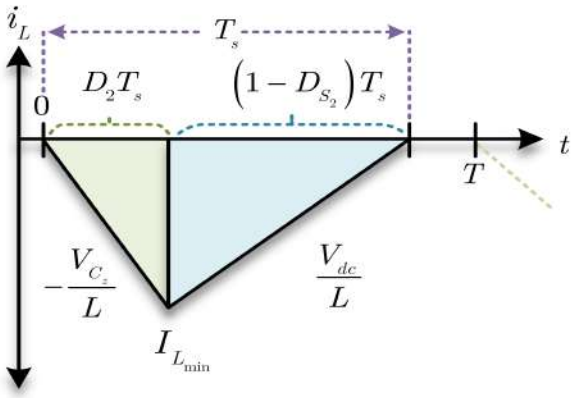
Figure 1.2. Switching operation during charging mode.



(a) $S_2 \rightarrow ON \rightarrow D_{S_2}T_s$ (third state).



(b) $S_2 \rightarrow OFF \rightarrow (1 - D_{S_2})T_s$ (fourth state).



(c) Current's evolution across the inductor during the third and fourth state.

Figure 1.3. Switching operation during discharging mode.

The average current across the inductor at the negative half-cycle can be determined as follows:

$$\begin{aligned} I_{L_{avg}}T_s &= \frac{1}{2}I_{L_{min}}(1-D_{S_2})T_2, \\ I_{L_{min}} = \frac{-V_{C_z}}{L}D_{S_2}T_s &= \frac{-V_{dc}}{L}(1-D_{S_2})T_2, \\ (1-D_{S_2})T_s &= \frac{-V_{C_z}}{V_{dc}}D_{S_2}, \\ I_{L_{avg}} &= \frac{V_{C_z}^2}{2LV_{dc}}D_{S_2}^2T_2. \end{aligned} \tag{1.4}$$

Similarly, the duty cycle for S_2 can be determined from Eq. 1.4:

$$D_{S_2} = \sqrt{\frac{2I_{L_{avg}} f_s L V_{dc}}{V_{C_z}^2}}. \tag{1.5}$$

1.3. Transfer inductor sizing

The transfer inductor is designed in DCM since it is not indispensable to keep a low current ripple across the inductor, thus the inductor value can be reduced.

For this analysis, the growth rate of the inductor current during the charging and discharging mode is considered (view Eqs. 1.2 and 1.4). In order to guarantee that the transfer inductor operates in DCM, the inductor should release all the stored energy in each switching cycle; that is:

$$T_1 + T_2 \leq T. \tag{1.6}$$

For the charging and discharging mode, Eq. 1.6 can be reformulated as:

$$\begin{aligned} D_{S_1} T_s \left(1 + \frac{V_{dc}}{V_{C_z}}\right) &\leq T, \\ D_{S_2} T_s \left(1 + \frac{V_{C_z}}{V_{dc}}\right) &\leq T. \end{aligned} \tag{1.7}$$

These two conditions must be satisfied when the ripple current reaches the rated maximum ripple current $I_{L_{max}}$. Eqs. 1.7 can become one as:

$$\frac{2I_{L_{max}} f_s L}{V_{dc}} \left(1 + \frac{V_{dc}}{V_{C_z}}\right) \leq T \tag{1.8}$$

Eq. 1.8 can be rewritten as:

$$\frac{L}{V_{dc}} \geq \frac{V_{C_z}^2}{2I_{L_{max}} f_s (V_{dc} + V_{C_z})^2}. \tag{1.9}$$

The maximum value of the inductor current ($I_{L_{max}}$) is presented at the peak value of the ripple current (view Eq. 1.10). Under this premise, it is possible to calculate the minimum value required of the transfer inductor.

$$I_{L_{max}} = \frac{I_{dc}}{D_{S_1}}, \tag{1.10}$$

where I_{dc} represents the DC-link average current for the rated power conditions.

Since the transfer inductor only fulfills the function of transferring energy, it is not necessary to obtain a strictly high performance in the current ripple, therefore a ripple no

greater than 1.5 times the maximum current in the inductor is defined by establishing two boundaries, one for the duty cycle of the switch S_1 and one for S_2 (1.11); these boundaries can be greater or lower depending of the desired maximum allowable current. In this case, the ripple is set by following the methodology in [40].

$$\begin{aligned} \frac{V_{dc}}{2L} D_{S_1} T &\leq 1.5 I_{L_{max}}, \\ \frac{V_{C_z}}{2L} D_{S_2} T &\leq 1.5 I_{L_{max}}. \end{aligned} \tag{1.11}$$

The first boundary of L can be determined from Eq. 1.11 as follows:

$$L \geq \frac{2 V_{dc} V_{C_z}^2}{9 I_{L_{max}} f_s (V_{dc} + V_{C_z})^2} = L_1. \tag{1.12}$$

For the second boundary, it is necessary to highlight that the inductor current must be restricted to be less or equal to the absolute maximum permissible value I_p. When the current across the inductor reaches its maximum value $I_{L_{max}}$ in one switching period, the second boundaries can be estimated as follows:

$$\begin{aligned} I_{L_{max}} + \frac{V_{dc}}{2L} D_{S_1} T &\leq I_p, \\ I_{L_{max}} + \frac{V_{C_z}}{2L} D_{S_2} T &\leq I_p, \end{aligned} \tag{1.13}$$

thus the second boundary for L, can be determined from Eq. 1.13 as follows:

$$L \geq \frac{V_{dc} I_{L_{avg}}}{2 f_s (I_p - I_{L_{max}})^2} = L_2. \tag{1.14}$$

Eqs. 1.12 and 1.14 implies that the inductor's value must be greater than the maximum value of L_1 and L_2, that is:

$$L > (L_1 \cup L_2). \tag{1.15}$$

1.4. Decoupling capacitor sizing

The decoupling capacitor for the Bidirectional Buck-Boost converter can be raised at first by the amount of ripple energy stored in the DC-link capacitor C_{dc} (view Fig. 1.4).

In a VSC (Voltage Source Converter) based system, the ripple energy stored in the DC-link can be determined by Eq. 1.16 [38].

$$E_r = \frac{V_{grid} I_{grid}}{\omega_0}, \tag{1.16}$$

where V_{grid} and I_{grid} are the *rms* grid and current voltages.

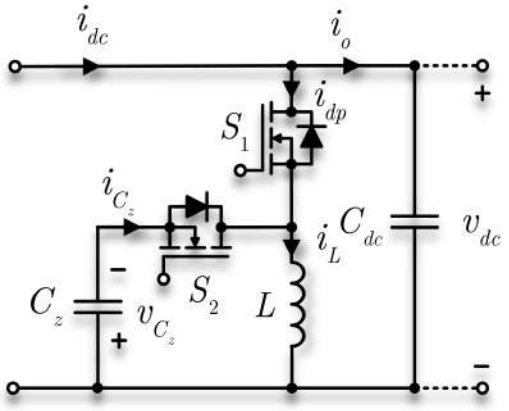


Figure 1.4. Bidirectional Buck-Boost converter with the DC-link capacitor.

The voltage ripple (peak-peak) across the DC-link capacitor C_{dc} can be determined as follows [13]:

$$\Delta V_{dc} \approx \frac{E_r}{C_{dc} V_{dc}}, \tag{1.17}$$

where V_{dc} is the average value of v_{dc}. It is clear from Eq. 1.17, that C_{dc} is inversely proportional to ΔV_{dc}, that is, the larger the DC-link capacitor the smaller the DC-link voltage ripple. In some power systems where a large DC-link voltage and a small voltage ripple are required, a very large DC-link capacitor is also demanded for guaranteeing the parameter's conditions. Nevertheless, this large capacitor implies several disadvantages such as low power density, efficiency, volume, and cost, among others [34].

The active power decoupling converter solves this problem by differing the DC-link ripple energy to the decoupling capacitor C_z, this way, the DC-link capacitor C_{dc} can be drastically reduced and film capacitors can be employed.

The voltage across the decoupling capacitor v_{C_z} has also a voltage ripple ΔV_{C_z}. In the same way that the energy in the DC-link capacitor was determined, the same principle can be applied to determine the size of the decoupling capacitor considering the energy it has to store (1.18).

The value of C_z can be determined in like manner the DC-link capacitor's value was determined; it has to be considered the energy that this capacitor has to store, and, at first, it is the same energy that C_{dc} stores, that is:

$$C_z \approx \frac{E_r}{\Delta V_{C_z} V_{C_z}}, \tag{1.18}$$

where ΔV_{C_z} and V_{C_z} are the voltage ripple (peak-peak) and the average voltage of the decoupling capacitor respectively. A relationship between the average voltage and the

ripple in this capacitor can be established through the Eq. 1.19.

$$r_z = \frac{\Delta V_{C_z}}{V_{C_z}}, \tag{1.19}$$

then the Eq. 1.18 can be rewritten as:

$$C_z \approx \frac{E_r}{r_z V_{C_z^2}}. \tag{1.20}$$

From the Eq. 1.20, it can be noticed that the decoupling capacitor C_z is inversely proportional to the square of the voltage level across it; that is, if the voltage on the decoupling capacitor is doubled, the capacitor can be reduced four times. If it is considered that the same energy E_r needs to be stored by the DC-link capacitor, the ripple voltage ratio across C_{dc} is:

$$r_{dc} \approx \frac{E_r}{C_{dc} V_{dc}^2}. \tag{1.21}$$

By combining the ripple voltage ratios of both capacitors, it can be determined how much the decoupling capacitor can be reduced in relation to the DC-link capacitor (1.22).

$$C_z \approx \frac{r_{dc}}{r_z} \left(\frac{V_{dc}}{V_{C_z}} \right)^2 C_{dc}. \tag{1.22}$$

1.5. Operation regions and power levels

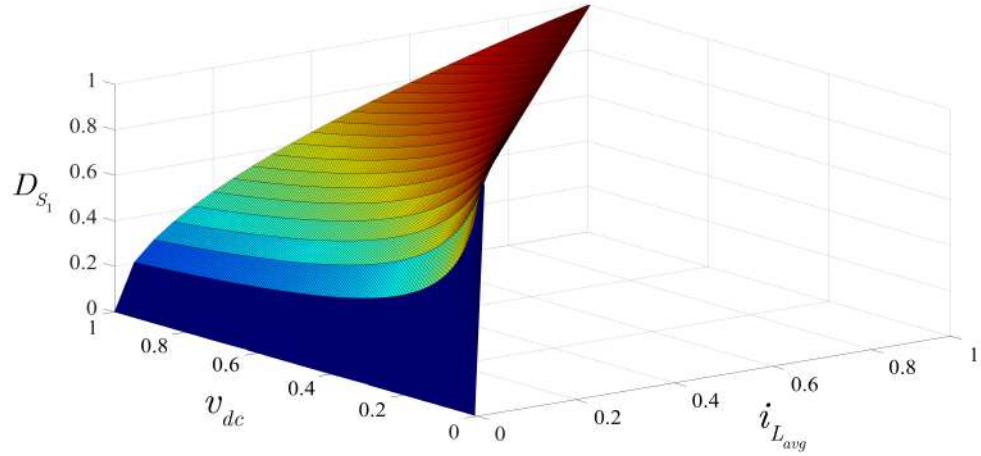
As discussed in section 2.1, the duty cycles D_{S_1} and D_{S_2} can be obtained from Eqs. 1.3 and 1.5. It must be noticed that these two equations contain square roots, then, the computation parameters must be restricted in order to avoid complex results or any indeterminacy. Considering this, it is possible to set boundaries for both D_{S_1} and D_{S_2} respectively,

$$\begin{aligned} 0 \leq & \sqrt{\frac{2 I_{L_{avg}} f_s L}{V_{dc}}} \leq 1, \\ 0 \leq & \sqrt{\frac{2 I_{L_{avg}} f_s L V_{dc}}{V_{C_z}^2}} \leq 1. \end{aligned} \tag{1.23}$$

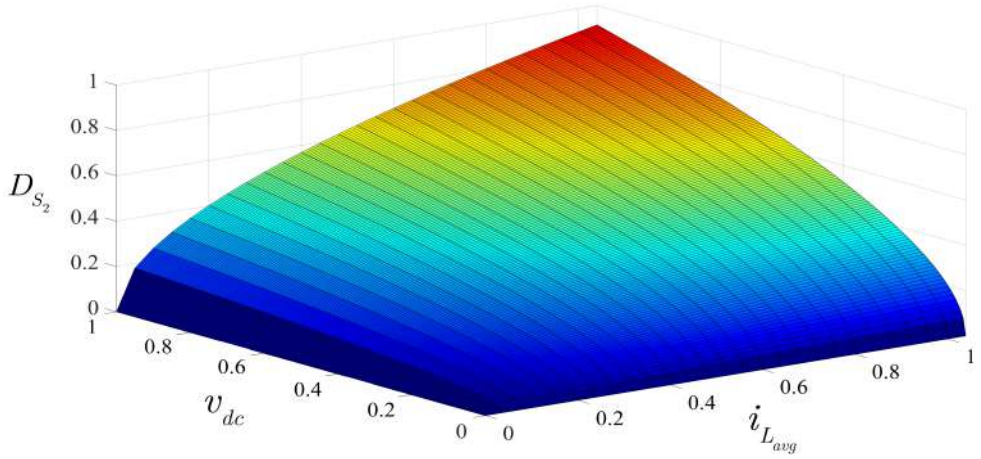
Figs. 1.5-(a) and (b) show the normalized operation regions for both duty cycles D_{S_1} and D_{S_2} respectively. It should be noticed that as the decoupling capacitor voltage is regulated by the control system, it can be considered as a constant value as well as the switching frequency f_s and the inductor L, then only the inductor current $I_{L_{avg}}$ and the

DC-link voltage V_{dc} are allowed to range, then $IL_{avg} \rightarrow iL_{avg}(t)$ and $V_{dc} \rightarrow v_{dc}(t)$. These considerations may change according to the control scheme.

It is important to remark that the operation regions can vary depending on every specific scenario setting, and Figs. 1.5-(a) and (b) only show a normalized example for view purposes.



(a) Operation region for D_{S_1}.



(b) Operation region for D_{S_2}.

Figure 1.5. Normalized operation regions for D_{S_1} and D_{S_2}.

In order to carry out simulation and experimental tests, it is necessary to define an equilibrium point of the converter for certain performance parameters. This allows an adequate sizing of the converter elements such as the transfer inductor, the decoupling capacitor, and the appropriate semiconductor devices selection. Table 1.2 shows the parameters selected for dimensioning the Bidirectional Buck-Boost Converter.

Table 1.2. Parameters for the Bidirectional Buck-Boost dimensioning.

Parameter	**Symbol**	**Value**	**Units**
Grid voltage	V_{grid}	48	V_{rms}
DC-link voltage	V_{dc}	100	V_{avg}
Ripple voltage on the DC-link	ΔV_{dc}	10	V_{pp}
Decoupling capacitor voltage	V_{C_z}	180	V_{avg}
Ripple voltage on the decoupling capacitor	ΔV_{C_z}	30	V_{pp}
Maximum allowed current across the inductor	I_p	5	A_p
Maximum allowed voltage on the power switches	$V_{S_{1max}}$	300	V
Maximum allowed current across the power switches	$I_{S_{1max}}$	5	A_p
Rated power	P_o	200	W
Load resistance	R_{load}	50	Ω
Switching frequency of Buck-Boost converter	f_s	50	kHz

First, a power level of $200W$ is defined. This power level is selected to carry out practical simulations and experimental tests at low power since the objective of these scenarios is just to validate the operating principle of the Bidirectional Buck-Boost converter as an active power decoupling scheme. The voltage level on the DC-link is defined at $100V$ with a voltage ripple of $10V_{pp}$; such values can vary depending on the desired DC-link voltage conditions. To guarantee the desired ripple voltage level at the DC-link terminals, it is necessary to guarantee an average voltage level in the decoupling capacitor of $180V$; this can be determined by following the capacitor sizing methodology and defining the maximum voltage levels of v_{dc} and v_{C_z}. It is important to remark that $V_{C_z} = 180V$ was defined by the limitations regarding the switch voltages; if there is no limitation, this voltage can be boosted as much as required.

For the transfer inductor, a first approximation to define the peak current is through the peak value of the current across the DC-link. However, according to the inductor sizing methodology, slightly higher current levels can be defined in order to oversize the inductor to operate against disturbances where the converter operates above the rated power. In this case, a peak current of no more than $5A$ is defined; this value can be determined at first by the DC-link average current, but the desired final inductance size can also be an important factor to take into account.

It is important to emphasize that the performance parameters must be defined considering the maximum voltage and current levels that the semiconductor devices must withstand. These levels can be deduced from the switching sequence of the converter (view Fig. 1.3-(a) and (c)). The maximum voltage in semiconductor devices is determined by the sum of the instantaneous voltage on the DC-link and the decoupling capacitor; i.e.:

$$V_{S_{1max}} = V_{dc_{max}} + V_{C_{z_{max}}}. \tag{1.24}$$

On the other hand, the maximum current that semiconductor devices must withstand is directly the maximum current in the transfer inductor; that is:

$$I_{S_{1_{max}}} = I_{L_{max}}. \tag{1.25}$$

1.5.1. Transfer inductor calculation

In order to propose a complete scheme of the Bidirectional Buck-Boost converter, it is necessary to raise an operation scenario to calculate the passive elements. The parameters in the Table 1.2 are proposed.

Considering the input/output voltage equation for a typical Buck-Boost converter, the required duty cycle in open-loop for the parameters raised is given by the following equation:

$$D_{S_1} = \sqrt{\frac{2I_{L_{avg}} f_s L}{V_{dc}}} = 0.6429. \tag{1.26}$$

The peak value of the current flowing across the transfer inductor can be then calculated as follows:

$$I_{L_{max}} = \frac{I_{dc}}{D_{S_1}} = 3.11A. \tag{1.27}$$

Considering the value obtained from the Eq. 1.27 and the parameters from Table 1.2, the two boundaries L_1 and L_2 can be determined:

$$\begin{aligned} L \geq \frac{2V_{dc}V_{C_z}^2}{9I_{L_{max}} f_s (V_{dc} + V_{C_z})^2} &= L_1 = 93.07\mu H. \\ L \geq \frac{V_{dc} I_{L_{avg}}}{2f_s (I_p - I_{L_{max}})^2} &= L_2 = 600\mu H. \end{aligned} \tag{1.28}$$

This means that the final inductor's value, L, must be greater than $600\mu H$.

1.5.2. Decoupling capacitor calculation

In order to estimate the value of the decoupling capacitor C_z, it is necessary to estimate the energy processed at first by the DC-link capacitor. The parameters used are shown in Table 1.2.

Considering a lossless system, the demanded power from the AC mains is the same as the supplied to the load, that is:

$$P_{in} = P_{out} = V_{grid} I_{grid} = V_{dc} I_{dc} = 200W. \tag{1.29}$$

where v_{grid} and i_{grid} are the *rms* grid voltage and current and V_{dc} and I_{dc} are the average voltage and current across the DC-link respectively.

The processed energy on the DC-link can be defined as in Eq. 1.30 while the required capacitance to hold this energy for the passive decoupling can be defined as in Eq. 1.31.

$$E_{dc} = \frac{V_{grid} I_{grid}}{w_0} = 0.53J. \tag{1.30}$$

$$C_{dc} = \frac{E_{dc}}{\Delta V_{dc} V_{dc}} \approx 530\mu F. \tag{1.31}$$

The decoupling capacitor can be easily estimated by finding the average voltage and ripple ratio for both the DC-link and decoupling capacitors as shown in Eqs. 1.32 and 1.33 respectively.

$$r_{dc} = \frac{\Delta V_{dc}}{V_{dc}} \times 100 = 10. \tag{1.32}$$

$$r_z = \frac{\Delta V_{C_z}}{V_{C_z}} \times 100 = 16.11. \tag{1.33}$$

The relationship between the DC-link capacitor and the decoupling capacitor (R_d)can be raised as follows:

$$R_d = \frac{\Delta V_{C_z} V_{C_z}}{\Delta V_{dc} V_{dc}} = 5.2. \tag{1.34}$$

The Eq. 1.34 shows the theoretical number of times the total capacitance required can be reduced with regard to the DC-link capacitor.

Finally, the decoupling capacitor can be computed as the number of times that the DC-link capacitance can be reduced, that is:

$$C_z \approx \frac{C_{dc}}{R_d} = 101\mu F. \tag{1.35}$$

1.6. Control system

A proper control system must be implemented for ensuring the performance of the power decoupling converter. As mentioned in section 2.1, the bidirectional Buck-Boost converter aims to drive the low-frequency oscillatory current (i_h) at $2\omega_0$ through the power decoupling stage. All this results in the following control requirements:

- The oscillatory component of current i_{dc} must be equal to i_{dp}.
- The average voltage v_{C_z} must be regulated at a certain voltage level to keep bounded the desired ripple voltage on the DC-link.

According to [39], there are essentially three well-known ways to perform the control strategy for the power decoupling converter. The first method consists of keeping the average voltage of v_{C_z} regulated to guarantee a determined average voltage on the DC-link and the ripple oscillations bounded. The second method consists in maintaining a determined relationship between the ripple voltage and the average voltage of v_{C_z}; that is, to regulate both the ripple voltage and the average voltage of v_{C_z} to guarantee the conditions of the ripple voltage on the DC-link. Finally, the third method consists of defining a minimum voltage level to guarantee the desired power ripple in the DC-link. The difference between this method and the first is that it seeks to reduce the voltage stress on the decoupling capacitor C_z and therefore on the power switches.

For the Bidirectional Buck-Boost converter, the first method is implemented because of its ease and simplicity of implementation; this control strategy is based on the work reported in [39] (view Fig. 1.6).

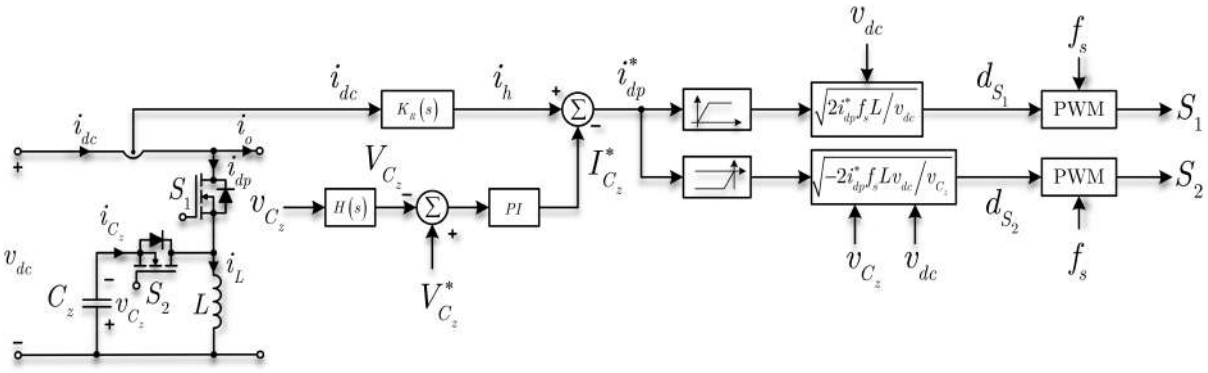


Figure 1.6. Control strategy for the Bidirectional Buck-Boost converter.

Initially, the current i_{dc} is measured; this current holds the oscillatory harmonic at $2\omega_0$, so, after being measured, this current is subjected to a resonant filter $K_{R(s)}$(view Eq. 1.36) which provides the $2\omega_0$ component only:

$$K_R(s) = \frac{2\xi h\omega_0 s}{s^2 + 2\xi h\omega_0 s + (h\omega_0)^2}, \tag{1.36}$$

where $h = 2$ and $\omega_0 = 2\pi f$. In order to cope with frequency variations, ξ can be selected as $0.01 - 0.02$ [39]. The behavior of the resonant filter can be illustrated in Fig. 1.7. It can be noticed from the latter that the harmonic at $120Hz$ is allowed to pass while the other frequency band is suppressed.

Subsequently, the average voltage of v_{C_z} can be obtained through a first-order Low-Pass filter (view Eq. 1.37). The bode diagram is shown in Fig. 1.8. Higher order filters could be used but it is not recommended because of the time delay that these could provide

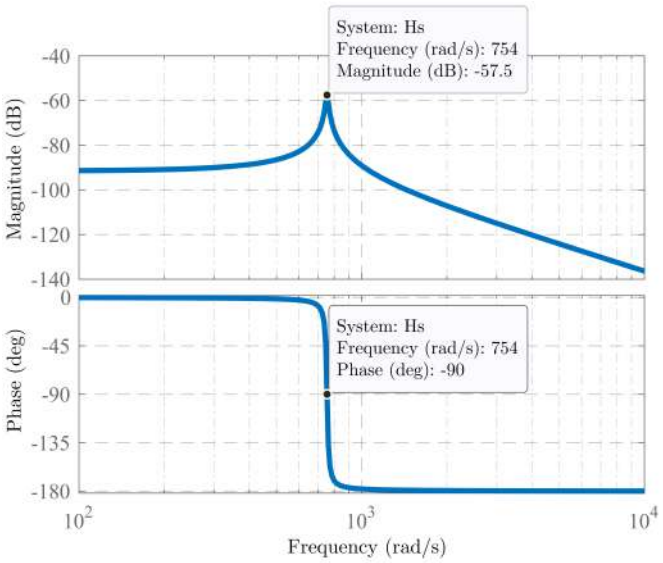


Figure 1.7. Bode diagram for the resonant filter $K_R(s)$.

when computing the average value.

$$H(s) = \frac{\omega_0}{s + \omega_0}. \tag{1.37}$$

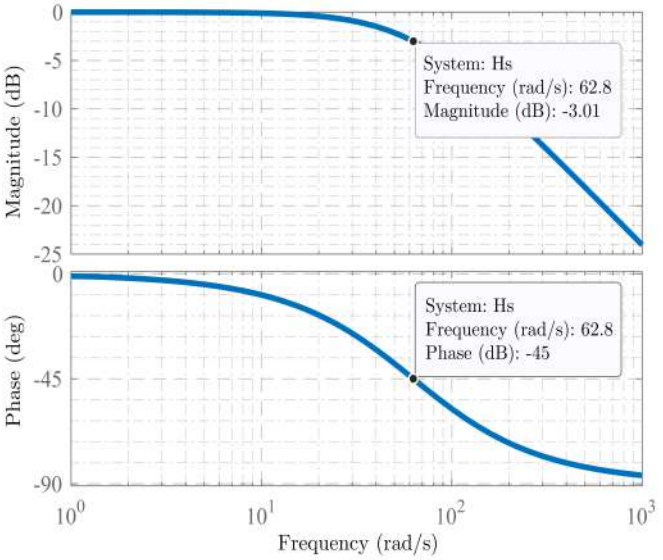


Figure 1.8. Bode diagram for the Low-Pass filter $H(s)$.

The average voltage V_{C_z} is compared with its reference and the error is subjected to a PI controller which provides the average capacitor current reference $I^*_{C_z}$; the subtraction of these two elements gives, as a result, the reference current i^*_{dp} which is used for calculating the duty cycle for each power switch (Eq. 1.5); it is important to remark the values for

the calculation of D_{S_1} and D_{S_2} must be strictly bounded for avoiding any indeterminacy. Finally, a constant PWM is implemented to turn on and off the power switches. The structure of the PI controller can be represented by the Eq. 1.38.

$$G_{PI}(s) = k_p \left(1 + \frac{1}{T_i s}\right), \tag{1.38}$$

where the controller tuning can be approximated with a gain k_p determined to reach the loop time T_i from $I^*_{C_z}$ to $V^*_{C_z}$, which approximates the following expression [39]:

$$k_p = \frac{C_z}{T_i}. \tag{1.39}$$

The reason why a PI control is implemented is due to its simplicity and practicality of implementation and tuning. In addition, considering the objectives and scope of this work, it is enough to implement this type of control in order to validate the operating principle of the converter. In addition, in [39, 41], it has been shown that the control system used operates adequately with a good performance.

CHAPTER 2

DC/AC CONVERTER WITH DEPENDENT ACTIVE POWER DECOUPLING FEATURE

A typical scheme for a single-phase DC/AC Full-Bridge based power converter or typically known as a *power inverter* interconnected to the electrical grid is the one shown in Fig. 2.1.

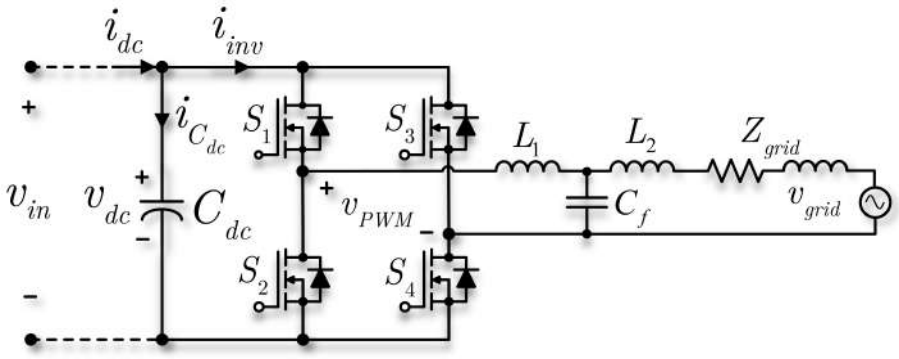


Figure 2.1. Typical DC/AC Full-bridge based power converter.

It is comprised of four power switches, $S_1 - S_4$. The switch pairs S_1, S_2 and S_3, S_4 conduct in turn and can be controlled under the same modulation strategy [42]. This power converter aims to map the energy on the DC-link and turn it into a sinusoidal waveform for supplying active power to the load or the AC mains. LC or LCL filters are implemented for removing high-frequency harmonics presented on the PWM voltage (v_{PWM}), guaranteeing the Total Harmonic Distortion (THD) required at the output [43]. During this conversion process, a voltage ripple on the DC-link is presented because of the alternating power supplied to the load. The typical structure for a DC/AC converter solves this issue by adding large electrolytic capacitors in the terminals of the DC-link. However, as discussed in the introduction chapter, the use of large electrolytic capacitors

implies several disadvantages, such as increased volume and weight, lower power density and efficiency, among others [15].

From the study carried out in the introduction chapter, it has been found that there exist several schemes for performing active power decoupling; however, the scheme reported in [24] has demonstrated outstanding performance according to the parameters raised in the comparative conducted.

In this chapter, a DC/AC power converter with an active power decoupling feature as an alternative to a regular single-phase DC/AC Full-Bridge based power converter is evaluated.

2.1. Operation principle

The DC/AC converter with a dependent active power decoupling is shown in Fig. 2.2. It initially bears resemblance to the original DC/AC Full-Bridge converter; it has four power switches ($S_1 - S_4$) and the switch pairs S_1, S_2 and S_3, S_4 also conduct in turn, nevertheless, they both meet a completely different task: switches S_1 and S_2 meets the task of performing active power decoupling and buffering the voltage ripple that is presented in the terminals of the PV system; that is, it transfers the ripple voltage presented in v_{in} through a transfer inductor L_b and this energy is then stored in the DC-link capacitor C_{dc}, thus the voltage in the PV system is constant and the ripple is reduced by allowing large voltage oscillations in v_{dc}. Since the ripple oscillations in the DC-link are not strictly requested to be small, then the minimum required capacitance can be drastically reduced. It is important to highlight that the active power decoupling stage stands for a bidirectional Boost converter.

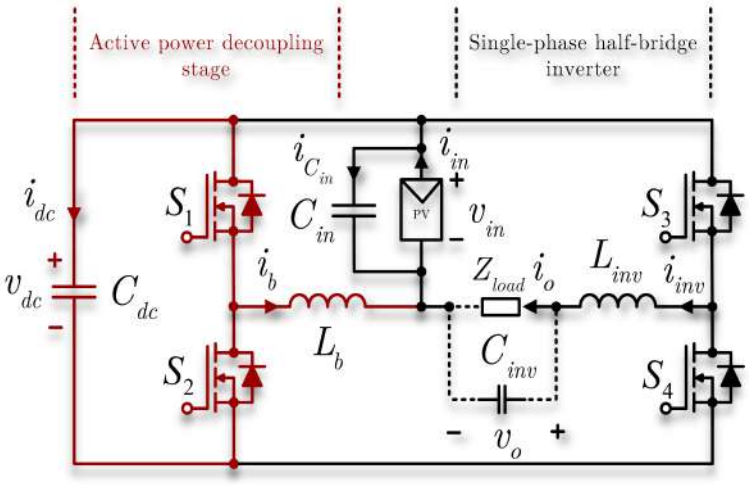


Figure 2.2. DC/AC converter scheme with active power decoupling feature operating as a forming converter.

The switches S_3 and S_4 meet the task of a single-phase half-bridge inverter; it aims to generate an AC bus for the local loads connected to it operating as a forming converter. However, it can also operate as a feeding converter which consists of mapping the energy generated by the PV system and supplying it to the grid. This operation mode is shown in Fig. 2.3. It has to be emphasized that even though this scheme has a different components arrangement, it can operate indeed as the traditional full-bridge structure shown in Fig. 2.1.

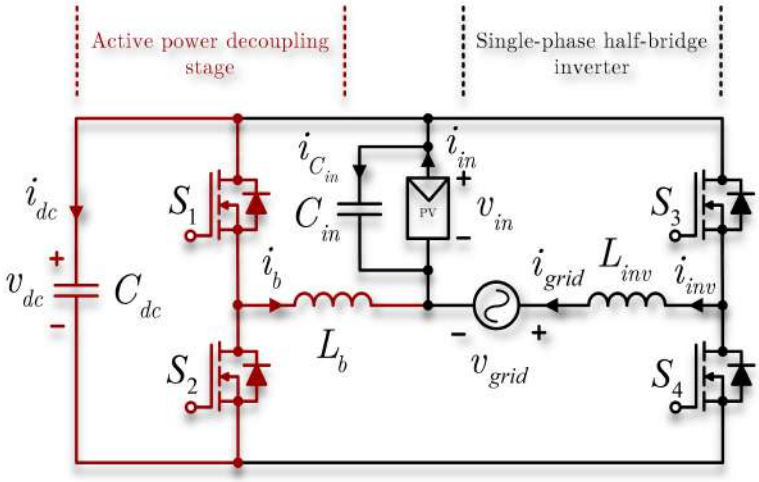


Figure 2.3. DC/AC converter scheme with active power decoupling feature operating as a feeding converter.

Considering the scheme shown in Fig. 2.3, the grid voltage and current v_{grid} and i_{grid} can be defined as follows:

$$\begin{aligned} v_{grid} &= V_p \sin(\omega_0 t), \\ i_{grid} &= I_p \sin(\omega_0 t + \theta). \end{aligned} \tag{2.1}$$

The instantaneous power supplied to the grid is given by Eq. 2.2.

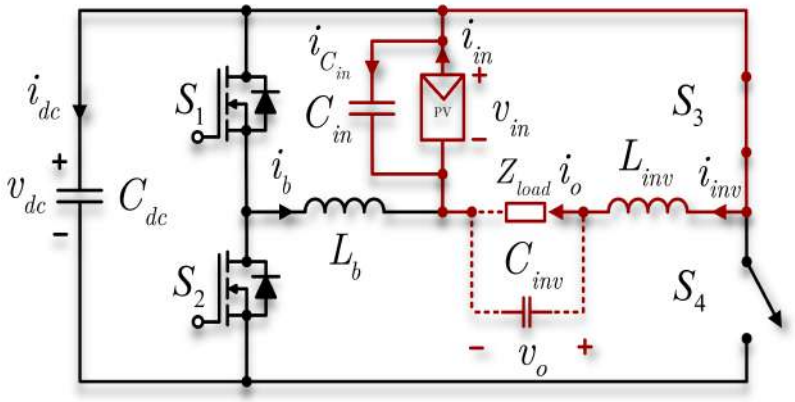
$$p_{grid} = v_{grid} i_{grid} = \frac{V_p I_p}{2} \left[\cos\theta - \cos(2\omega_0 t + \theta)\right]. \tag{2.2}$$

It can be observed from Eq. 2.2 that the instantaneous output power is composed of two terms: the average power $V_p I_p/2$, which is constant, and a second term given by $\cos\theta - \cos(2\omega_0 t + \theta)$ which oscillates at twice the grid's frequency with an amplitude of the average power supplied at the output of the inverter. As mentioned above, the DC-link voltage holds the same 2nd harmonic presented in p_{grid} and this can be represented as follows:

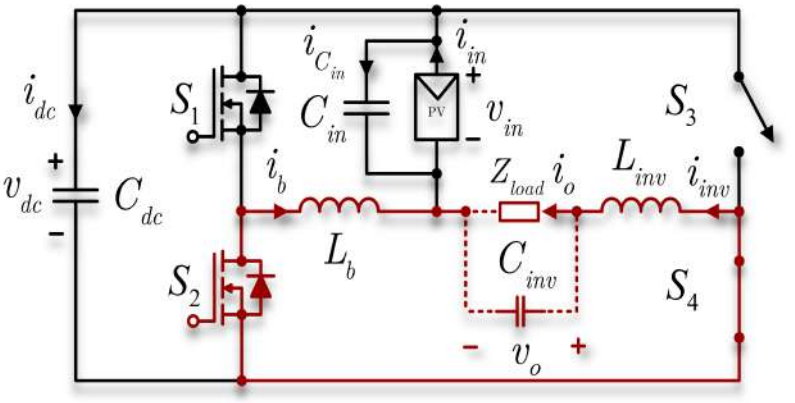
$$v_{dc} = V_{dc} + V_r \sin(2\omega_0 t + \theta), \tag{2.3}$$

where V_r is the peak ripple voltage.

Looking at the forming operation mode shown in Fig. 2.2, when the switch S_3 is on and S_4 off, the output voltage is given by the PV system voltage, that is $v_o = v_{in}$ (view Fig. 2.4-(a)). On the other hand, when S_4 is on and S_3 off, the output voltage is given by the subtraction of v_{in} and v_{dc}; that is $v_o = v_{dc} - v_{in}$ (view Fig. 2.4-(b)). This particular characteristic is imposed by the fact that the negative terminal of the PV system is directly connected to the neutral terminal of the output load/ electrical grid and this, at the same time implies an important advantage because of the reduction of the common mode leakage currents that are commonly presented in transformer-less PV inverters [24].



(a) First mode $S_3 \rightarrow ON$.



(b) Second mode $S_4 \rightarrow ON$.

Figure 2.4. Operation modes of the DC/AC forming converter with active power decoupling feature.

Although this scheme represents outstanding advantages, it has to be highlighted that has some limitations and restrictions because of its configuration structure; these

restrictions can be formulated from the approach obtained by Fig. 2.4 as follows:

$$\begin{aligned} &\text{If } v_o(t) \geq 0,\ v_{in}(t) > v_o(t), \\ &\text{If } v_o(t) < 0,\ v_{dc}(t) - v_{in}(t) > v_o(t). \end{aligned} \tag{2.4}$$

From the Eq. 2.4, it can be observed that these restrictions represent important drawbacks because when the general operation of a Half-Bridge inverter is considered, the maximum input voltage has to be greater than the peak value of the sinusoidal signal at the inverter output. However, since the input voltage consists of the subtraction of $v_{dc} - v_{in}$ and, in addition to this, the voltage v_{dc} contains the oscillatory harmonic at $2\omega_0$, it must be guaranteed that this subtraction is always greater than the peak value of the desired sinusoidal signal at the inverter output, which also implies guaranteeing certain voltage levels in v_{dc} and v_{in}.

In general terms, the complete operation of the converter consists that through the half-bridge inverter stage, a sinusoidal signal is reproduced at the output for supplying active power to the load or the grid at issue, while the active decoupling conversion stage is responsible for buffering the oscillations present in the terminals of the photovoltaic system. It should be then highlighted that the switches S_1 and S_2 are controlled independently of the switches S_3 and S_4 since both of them have completely different tasks. From the approach of Fig. 2.4 and the Eqs. 2.1, 2.3 and 2.4 and considering that the modulation signals for both the active power decoupling and the inverter stages (m_b and m_{inv} respectively) must be restricted as follows:

$$\begin{aligned} 0 <& m_b < 1, \\ 0 <& m_{inv} < 1, \end{aligned} \tag{2.5}$$

where the modulation waveforms for both stages can be determined by the Eqs. 2.6 and 2.7 respectively.

$$m_b = \frac{V_{dc} - V_{in} + V_r \sin(2\omega_0 t + \theta)}{V_{dc} + V_r \sin(2\omega_0 t + \theta)}. \tag{2.6}$$

$$m_{inv} = \frac{V_{dc} - V_{in} + V_p \sin(\omega_0 t) + V_r \sin(2\omega_0 t + \theta)}{V_{dc} + V_r \sin(2\omega_0 t + \theta)}. \tag{2.7}$$

It can be observed from Eqs. 2.6 and 2.7, that the modulation waveforms for both active decoupling and inverter stages are not constant and purely sinusoidal respectively as in traditional Boost and Full-Bridge converters are expected. For Eq. 2.6, the second order harmonic at $2\omega_0$ is added to m_b for buffering this component present in v_{in} and divert it to v_{dc}. In m_{inv}, the harmonic $2\omega_0$ component is also included for reducing its effect at the output voltage of the Half-Bridge inverter.

In summary, the converter considerations and remarks are listed below:

1. Large ripple oscillations in v_{dc} are allowed in order to keep v_{in} constant.
2. The average value of v_{in} must be greater at all times than the peak value of v_o in order to guarantee the output voltage parameters. Likewise, $v_{dc}(t) - v_{in}(t) > v_o(t)$.
3. The minimum DC-link voltage required is imposed by the output and the PV system voltages, that is: $v_{dc} \geq -V_p \sin(\omega_0) + v_{in}$.
4. The pairs of branches S_1, S_2 and S_3, S_4 operate individually and both are controlled by two different modulation waveforms (m_b and m_{inv}).
5. Neither m_b nor m_{inv} must be necessarily pure constant and sinusoidal waveforms respectively, since both of them hold the $2\omega_0$ harmonic. However, they are bounded for operating in the linear region; that is $0 < m_b < 1$ and $0 < m_{inv} < 1$.

2.2. Decoupling capacitor sizing

In order to determine the appropriate value of the decoupling capacitor C_{dc}, it is necessary to consider the energy that is intended to be processed in the DC-link. This energy is given by the following expression:

$$p_{dc} = \frac{d}{dt} E_{dc} = \frac{1}{2} \frac{d}{dt} \left[C_{dc} v_{dc}^2(t) \right]. \tag{2.8}$$

If the derivative is applied as shown in Eq. 2.8, the following expression is obtained:

$$p_{dc} = \omega_0 C_{dc} \left[2 V_{dc} V_r \cos(2\omega_0 t + \theta) + V_r^2 \sin(4\omega_0 t + 2\theta) \right]. \tag{2.9}$$

By combining the Eqs. 2.2 and 2.9, Eq. 2.10 is then obtained, which illustrates the minimum capacitance required in the DC-link to guarantee the power requirements.

$$C_{dc} = \frac{V_p I_p}{4\omega_0 V_{dc} V_r}. \tag{2.10}$$

2.3. LC filter sizing

The DC/AC Half-Bridge inverter requires a low-pass filter in order to remove the high-frequency harmonics presented on the switching voltage v_{pwm}. The general principle of the filter is to take advantage of a low-pass behavior with *Butterworth* response to attenuate the high-frequency harmonics that the switched voltage signal of the inverter output holds, in such a way that at the filter's output, only the fundamental harmonic at ω_0 is allowed

to pass, obtaining, as a consequence, a completely sinusoidal waveform; it is important to highlight that the filter's approach is intended for the forming configuration but it is still useful for the feeding mode. Fig. 2.5 shows the behavior of the second-order low-pass filter with a *Buterrworth-type* response with an attenuation of $-3dB$ at the desired cutoff frequency f_c, where it can be seen that the high-order harmonics at m_f and $2m_f$ are removed.

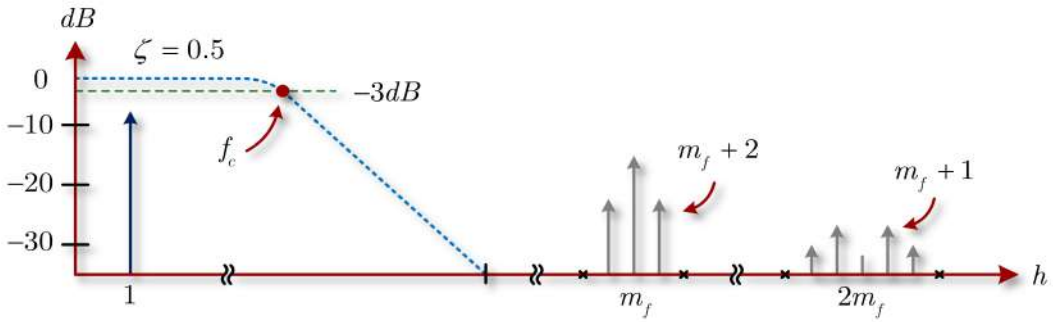


Figure 2.5. Representation of the SPWM Half-Bridge inverter harmonic content with a second-order low-pass filter.

The equivalent representation of the inverter output voltage and the LC filter is shown in Fig. 2.6.

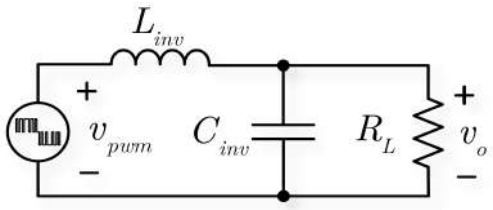


Figure 2.6. Equivalent circuit for the Half-Bridge output voltage and the LC filter.

The frequency response of the circuit from Fig. 2.6 with a purely resistive load can be obtained as follows:

$$H\left(j\omega\right) = \frac{v_o}{v_{pwm}} = \frac{1}{L_{inv}C_{inv}\left(j\omega\right)^2 + \frac{L}{R_L}j\omega + 1}. \tag{2.11}$$

The typical second-order transfer function can be then obtained from Eq. 2.11 as follows:

$$H\left(j\omega\right) = \frac{v_o}{v_{pwm}} = \frac{1}{\frac{1}{\omega_c^2}\left(j\omega\right)^2 + \frac{2\zeta}{\omega_c}j2\omega + 1}. \tag{2.12}$$

where ω_c is the filter's cutoff frequency and ζ is the damping factor. Both of them can be estimated in Eqs. 2.13 and 2.14 respectively.

$$\omega_c = \frac{1}{\sqrt{L_{inv}C_{inv}}}. \tag{2.13}$$

$$\zeta = \frac{\sqrt{L_{inv}/C_{inv}}}{2R_L}. \tag{2.14}$$

where the angular cut-off frequency ω_c can be also expressed in degrees as $f_c = \omega_c/2\pi$. The filter's characteristic impedance can be expressed as follows:

$$Z_L = \sqrt{\frac{L_{inv}}{C_{inv}}}. \tag{2.15}$$

Then, the Eq. 2.14 can be redefined as:

$$\zeta = \frac{1}{2}\left(\frac{Z_L}{R_L}\right). \tag{2.16}$$

If the damping factor is selected as $\zeta = 0.5$ in order to obtain a plane response and considering $f_c \geq 10f_1$, then the equations for both L_{inv} and C_{inv} can be deducted as follows:

$$C_{inv} = \frac{1}{10\left(2\pi f_1\right) R_{L_{min}}}, \tag{2.17}$$

$$L_{inv} = \frac{R_{L_{min}}}{10\left(2\pi f_1\right)}, \tag{2.18}$$

where $R_{L_{min}}$ and f_1 are the minimum equivalent resistance for the maximum power to be supplied to the load and the fundamental harmonic frequency respectively.

It is important to remark that the grid voltage v_{red} is assumed dominant when the converter operates in feeding mode; furthermore, the filter's cut-off frequency is set for at least ten decades higher than the fundamental frequency in order to keep a low THD_i in i_{inv}. The cut-off frequency can be set by the following equation:

$$10f_1 < f_c < \frac{\left(2m_f - 5\right) f_1}{10}, \tag{2.19}$$

where m_f is the frequency index modulation given by f_s/f_1.

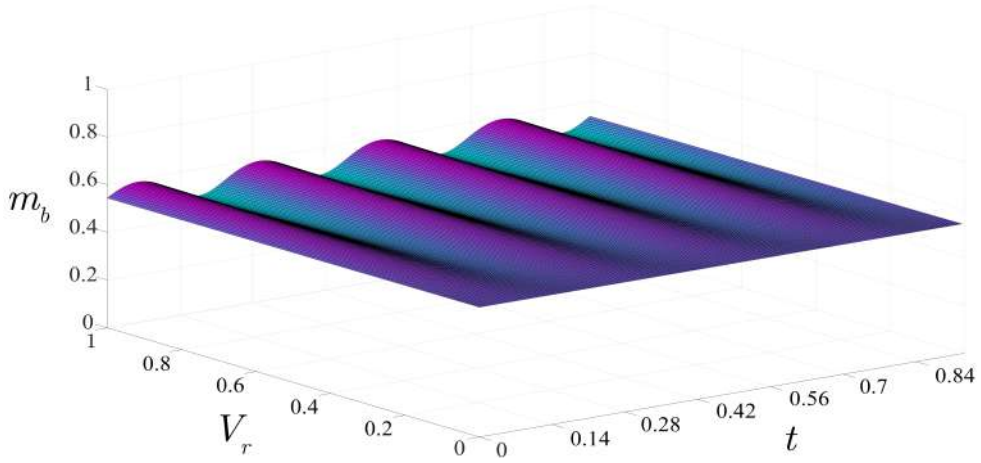
2.4. Operation regions and power levels

As discussed in section 2.1, the modulation indices m_b and m_{inv} can be obtained from Eqs. 2.6 and 2.7. It is important to remark that in order not to take the converter to an invalid operating point, it is necessary to guarantee that the duty ratios are limited as follows:

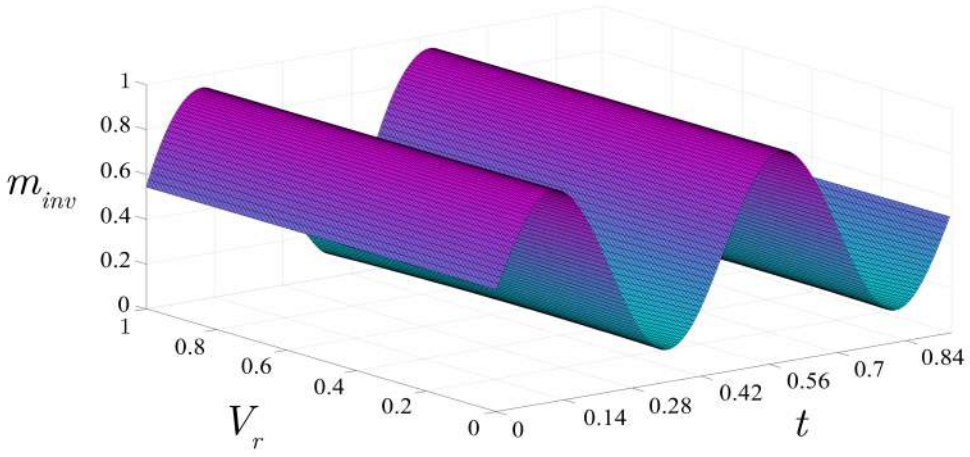
$$0 < \frac{V_{dc} - V_{in} + V_r \sin\left(2\omega_0 t + \theta\right)}{V_{dc} + V_r \sin\left(2\omega_0 t + \theta\right)} < 1, \tag{2.20}$$

$$0 < \frac{V_{dc} - V_{in} + V_p \sin(\omega_0 t) + V_r \sin(2\omega_0 t + \theta)}{V_{dc} + V_r \sin(2\omega_0 t + \theta)} < 1. \tag{2.21}$$

Since in a closed-loop scenario the average value of the DC-link voltage and the voltage in the photovoltaic system are controlled parameters, it can be assumed that both parameters are constant in steady-state. In addition, it is known that the voltage of the electrical grid is fixed and invariable since it is considered an ideal grid. The only parameter that can vary freely is the ripple voltage on the DC-link since it increases or decreases depending on the amount of ripple energy that exists at the terminals of the photovoltaic system. If a variation of $50V_{pp}$ is considered, then the characteristic curves of the operating points for both m_b and m_{inv} can be computed as in Figs. 2.7-(a) and (b) respectively.



(a) Operation region for m_b.



(b) Operation region for m_{inv}.

Figure 2.7. Normalized operation regions for m_b and m_{inv}.

In Fig. 2.7-(a) can be seen that as long as the peak value of the DC-link ripple voltage (V_r) is null, the duty ratio m_b remains practically constant for each lapse interval. However, as the ripple voltage increases, the harmonic at $2\omega_0$ shows up in m_b, causing larger oscillations and extending minimum and maximum values. Fig. 2.7-(b) shows the modulation index m_{inv}, in which it is observed that the signal remains bounded between 0 and 1 even though the ripple voltage grows. When the ripple voltage increases, the harmonic at $2\omega_0$ becomes more noticeable in order to reduce its effect on the inverter output.

These figures illustrate the modulation waveforms changes when the ripple voltage on the PV system increases or decreases. It must be remarked that they were only shown for visualization purposes and it is important to be aware of the maximum and minimum bounds of the parameters that govern the values of m_b and m_{inv} for every specific scenario, since these parameters can vary and are important to set the minimum and maximum values that the duty ratios can reach; this allows preventing the converter from operating in the overmodulation region.

In order to carry out simulation and experimental tests, it is necessary to define an equilibrium point of the converter for certain performance parameters. This allows an adequate sizing of the converter elements such as the LC filter, the decoupling capacitor, and the appropriate semiconductor devices selection. Table 2.1 shows the parameters selected for dimensioning the DC/AC converter with the dependent active power decoupling feature.

Table 2.1. Parameters selected for dimensioning the DC/AC converter with the dependent active power decoupling feature.

Parameter	**Symbol**	**Value**	**Units**
Grid voltage	V_{grid}	127	V_{rms}
DC-link voltage	V_{dc}	450	V_{avg}
Ripple voltage on the DC-link	V_r	50	V_p
PV system voltage	V_{in}	205	V_{avg}
Grid frequency	f_1	60	Hz
Minimum load resistance	$R_{L_{min}}$	32.2	Ω
Filter damping	ζ	0.5	-
Rated power	P_o	500	W
Switching frequency	f_s	50	KHz
Cutoff frequency	f_c	5.1	KHz
Maximum allowed voltage on the power switches	$V_{Q_{max}}$	500	V
Maximum allowed current across the power switches	$I_{L_{b_{max}}}$	15	A_p

In the first instance, an output voltage of $127V_{rms}$ is defined. Afterward, the average value of the DC-link voltage is set to $450V$ with a ripple voltage of $50V_{pp}$. The average value

of the PV system is set to $205V$. It is important to remark that these voltage levels are initially defined by the restrictions of Eqs. 2.4 and the operation considerations addressed in section 2.1 and considering that $v_{dc} \geq -V_p \sin(\omega_0) + v_{in}$.

For the dimensioning of the LC filter, a cutoff frequency of $5.1kHz$, a switching frequency of $50kHz$, and a damping factor of 0.5 are considered to obtain a response as close as possible to the Butterworth-type response.

In order to size the semiconductor devices, the maximum voltage on the DC-link and the maximum current across the inductors L_b and L_{inv} are taken into account; it is important to emphasize that the current flowing through these two inductors is different, then the maximum current of both inductors is taken into account and the largest one is chosen. Knowing that:

$$\begin{aligned} V_{Q_{max}} &= V_{dc_{max}}, \\ I_{Q_{max}} &= I_{L_{b_{max}}}, \end{aligned} \tag{2.22}$$

it can be concluded that the power switches must be selected based on the maximum value of current across L_b and the peak value of the DC-link voltage.

2.4.1. Decoupling capacitor calculation

In order to estimate the value of the decoupling capacitor C_{dc}, the parameters of Table 2.1 are proposed. Then, based on the Eq. 2.10, C_{dc} can be calculated as follows:

$$C_{dc} = \frac{V_p I_p}{4\omega_0 V_{dc} V_r} \approx 29.42\mu F. \tag{2.23}$$

2.4.2. LC filter calculation

According to the methodology presented in the previous section, the parameters in the Table 2.1 are proposed to perform the calculation of the LC filter of the Half-Bridge inverter.

By using a large enough switching frequency, the output filter can be substantially reduced. For this application, a switching frequency of 50kHz is employed. This allows to increase the filter's cutoff frequency and thus reduce the value of L_{inv} and C_{inv}.

$$C_{inv} = \frac{1}{f_c (2\pi f_1) R_{L_{min}}} \approx 0.967\mu F, \tag{2.24}$$

$$L_{inv} = \frac{R_{L_{min}}}{f_c (2\pi f_1)} \approx 1mH. \tag{2.25}$$

2.5. Modeling and control system

In order to find an approximation of the average model of the converter shown in Fig. 2.3, the concept of *power poles* [44] is used, which consists of representing a branch of two switches through an ideal transformer with a transformation ratio equal to the instantaneous modulation signal; however, for the simulation implementation, it is also possible to use a model based on current and voltage-dependent sources. It should be noted that in order to obtain a more simplified version of the model, an ideal operation of the power switches is taken into account and a lossless system is assumed; regardless of the model simplification, it is still possible to study the converter's behavior with enough accuracy for the purposes raised, however, it is recommended to extrapolate the converter analysis under a deeper and more extensive model's representation by considering parasitic elements. The average representation of the power converter is shown in Fig. 2.8.

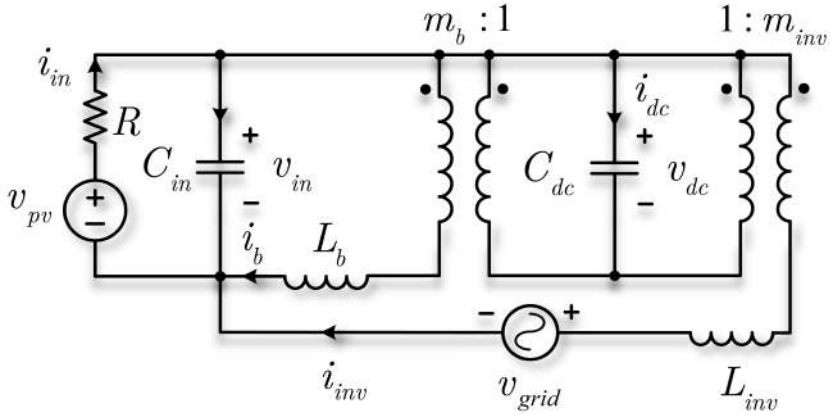


Figure 2.8. Converter's average model representation.

It is important to highlight that this control system is applied to the feeding mode of the power converter. To emulate the operation of the photovoltaic panel, it is modeled through an independent voltage source v_{pv} in series with a resistance R that provides a current (i_{in}), this way, the panel is emulated as a current source, which is defined through Eq. 2.26.

$$i_{in} = \frac{V_{pv} - v_{in}}{R}. \tag{2.26}$$

The average model of Fig. 2.8 can be obtained through the voltage and current

Kirchhoff's laws as shown in the set of equations in 2.27.

$$\begin{aligned} L_b \frac{di_b}{dt} &= v_{in} - m_b v_{dc}, \\ L_{inv} \frac{di_{inv}}{dt} &= -v_{in} - v_{grid} - m_{inv} v_{dc}, \\ C_{in} \frac{dv_{in}}{dt} &= i_{in} - i_b - i_{inv}, \\ C_{dc} \frac{dv_{dc}}{dt} &= m_{inv} i_{inv} + m_b i_b. \end{aligned} \tag{2.27}$$

The overall control objectives are listed below:

1. Regulate the PV voltage system v_{in} and operate in the Maximum Power Point (MPP).
2. Regulate the average voltage of v_{dc} and keep the ripple variations bounded.
3. Keep the inverter's output current regulated for supplying the active power available in the PV system to the electrical grid.

From the set of equations in 2.27, the control loops for the entire converter can be defined (view Fig. 2.9). The control strategy used is based on the work reported in [24].

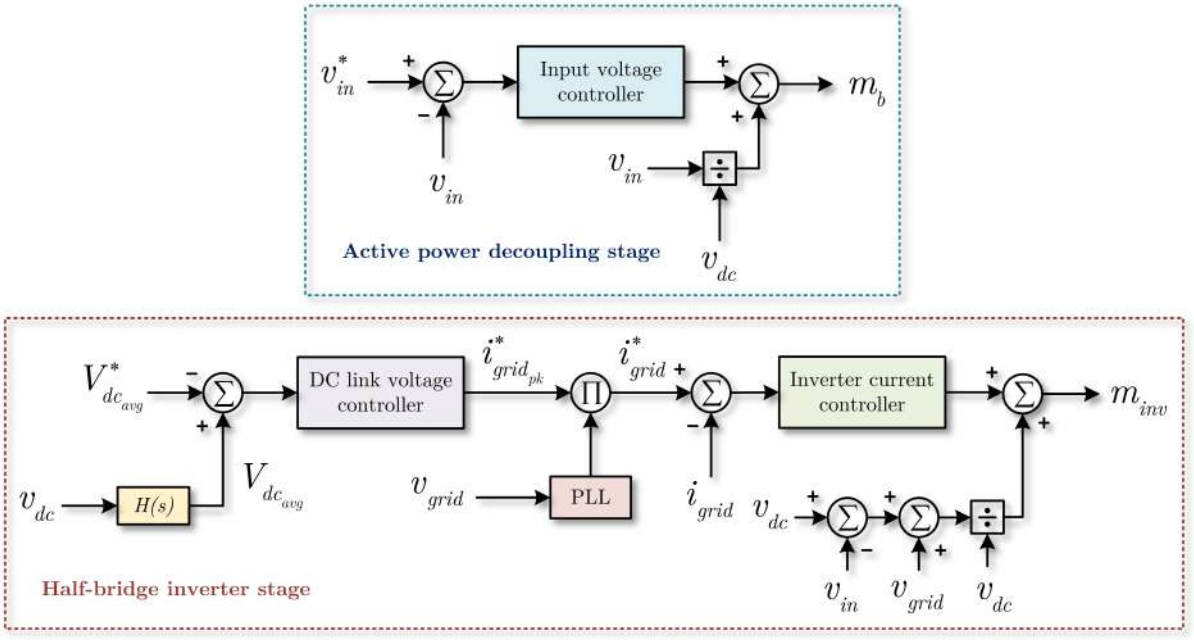


Figure 2.9. Converter control loops.

According to Fig. 2.9, the control system is made up of two different control loops. The first corresponds to the active power decoupling loop and aims to keep regulated the

PV system voltage and operate at the MPP. The second loop corresponds to the half-bridge inverter. This is composed of two sub-loops: the DC-link voltage and the inverter output current regulation. For the DC-link regulation, the average value of v_{dc} is first estimated; this is achieved by subjecting the voltage measurement to a Low-Pass Filter H_s. This filter's output is subtracted with the value of the average reference and the error is submitted to the DC-link voltage controller, which outputs the peak current reference needed to keep it regulated at a reference value. This peak value is multiplied by the reference offered by the Phase Lock Loop (PLL), the result is compared with the current measured at the inverter output and is submitted to the current controller that finally offers the modulation signal m_{inv} which is subjected to SPWM modulation to control the power switches. The input voltage, DC-link voltage, and inverter current controllers are PI controllers and their structure is shown in the Eq.2.28. The reason for using these controllers is due to the simplicity of implementation; besides, it is more than enough to use this type of controller to study the operating principle of the converter in closed-loop mode.

$$G_{PI}(s) = k_p \left(1 + \frac{1}{T_i s}\right), \tag{2.28}$$

where k_p and T_i are the proportional constant and the time of the integral action of the PI controller respectively.

2.5.1. Phase-Locked Loop *PLL*

In order to guarantee the power exchange between the Half-Bridge inverter and the electrical grid, it is vital to keep a sync between the inverter's output voltage and the grid's voltage for being able to supply active power; this means that both inverter and grid's angles must be as even as possible. A Phase-Locked Loop is then required for carrying out this task.

A Phase Locked Loop (PLL) is a closed loop system in which an internal oscillator is controlled to keep in sync with some external periodic signal using a feedback loop. According to [45], there exists numerous schemes for performing a PLL, nevertheless, in [43], it is shown that the PLL based on the Second-Order Generalized Integrator (*PLL SOGI*) demonstrates good performance for grid-interconnected applications.

The basic structure of a PLL SOGI is shown in Fig. 2.10.
where:

- v_{grid} is the measurement of the electrical grid voltage.
- v_{grid}^{α} is the filtered signal of the electrical grid.

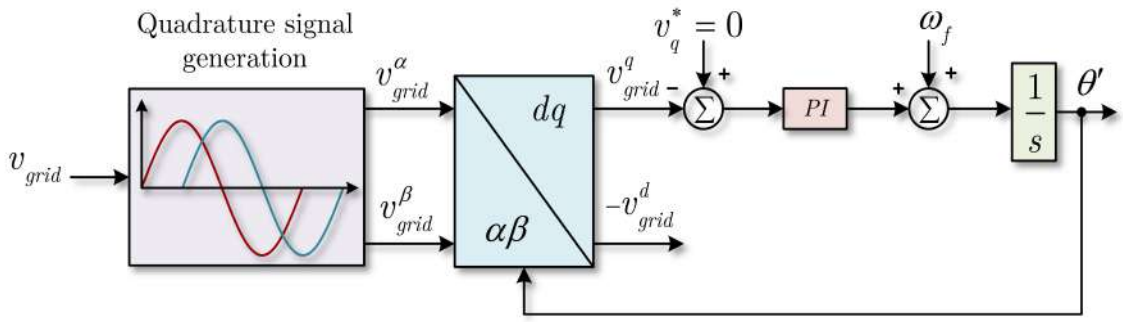


Figure 2.10. PLL based on the Second-Order Generalized Integrator.

- v^{β}_{grid} is the quadrature signal generated by the second-order generalized integrator.
- θ' is the reference angle for the electrical grid shifted $-\pi/2$.

Initially, the PLL SOGI is composed of four different stages: the quadrature signal generation, the dq transformation, a filter stage, and the phase angle generation. The quadrature signal stage produces a phase shift in the input signal v_{grid}. The dq transformation consists of a mapping of the rotating quadrature plane; that is, it turns a rotating frame signal into a constant frame. The main advantage of this transformation is the mapping of the fundamental signals in a DC component, being easier to apply control over them [46]. The filter stage can be performed by a PI controller, however, it can also be carried out by a typical low-pass filter. The angle generation can be performed by an external resettable integrator.

The quadrature signal generation is carried out by a Second-Order Generalized Integrator shown in Fig. 2.11. This system provides the required phase shift for the dq transformation. This block is composed of two resonant filters at the grid's frequency, from which two signals with similar characteristics are obtained; the first is the grid's filtered voltage in phase with the original signal v^{α}_{grid}, and the second is the grid's filtered voltage with a phase shift of $90°(v^{\beta}_{grid})$. The resonant filters are represented in Eqs. 2.29 and 2.30.

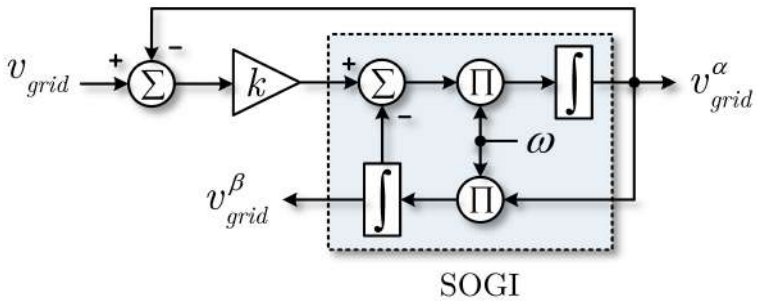


Figure 2.11. Second-Order Generalized Integrator structure.

$$G_\alpha(s) = \frac{k\omega s}{s^2 + k\omega s + \omega^2}, \tag{2.29}$$

$$G_\beta(s) = \frac{k\omega^2}{s^2 + k\omega s + \omega^2}, \tag{2.30}$$

where:

- k is a gain that reduces the filter's convergence time.
- k is the grid's angular frequency.

2.5.2. *dq* synchronous reference frame in PLL

The transformation *dq0* is a derivation of the Park transform also known as the synchronous reference frame transformation, which consists of a mapping of a time-varying system *abc* to a constant reference frame *dq0*. It is widely used in the study of electrical machines and control either in single-phase or three-phase systems [46].

The *dq0* transformation has its single-phase version, which requires the construction of an orthogonal system in order to obtain the *dq0* components; that is, a phase shift of 90° between the voltage and currents is required [47].

The *dq* transformation is essential for mapping the rotating frame signals obtained from the SOGI and turning them into the *dq* frame. The matrix employed for the *dq* transformation is shown in Eq. 2.31.

$$\begin{bmatrix} v_{grid}^d \\ v_{grid}^q \end{bmatrix} = \begin{bmatrix} \cos(\theta') & \sin(\theta') \\ -\sin(\theta') & \cos(\theta') \end{bmatrix} \begin{bmatrix} v_{grid}^\alpha \\ v_{grid}^\beta \end{bmatrix}. \tag{2.31}$$

It is important to highlight that the angle reference generated by the PLL is shifted 90° and it is necessary to adjust it when calculating the sinusoidal reference, that is:

$$\theta = \theta' - \frac{\pi}{2}. \tag{2.32}$$

2.5.3. PI controller for the PLL

The PI control aims to guarantee $v_q^* = 0$. The comparison between $v_{grid}^q = 0$ and $v_q^* = 0$ is due to the fact the scheme under study is a single-phase system and v_q must be strictly zero. In other words, it estimates the deviation in the grid's angular frequency, and when the central angular frequency is added, the grid's angular frequency is obtained. Subsequently,

this is subjected to an integrator that restarts every 2π and provides the phase angle θ' at the output. The transfer function of the PI control used in the PLL is defined as follows:

$$G_{PI_{PLL}}(s) = k_{p_{PLL}} \left(1 + \frac{1}{T_{i_{PLL}} s}\right). \tag{2.33}$$

Considering the tuning remarks in [45], the PI gains can be approximated as follows:

$$k_{p_{PLL}} = \frac{9.2}{t_s}, \tag{2.34}$$

$$T_{i_{PLL}} = \frac{t_s \xi^2}{2.3}, \tag{2.35}$$

where:

- t_s is the PLL's stabilization time.
- ξ is the damping constant.

2.5.4. Low-Pass filter for average value estimation

In order to obtain the average value of the DC-link voltage, it is necessary to submit the measurement to a filter process in which it is possible to get rid of the $2\omega_0$ harmonic, and only the average value is then obtained at the filter's output. To perform this process, the use of a first-order low-pass filter is employed and it is tuned to a low enough frequency of at least ten times lower than the cutoff frequency. The equation that represents the low-pass filter is shown in Eq. 2.36, where the attenuation of $-3dB$ is reached at $10Hz$ with a *Butterworth* response.

$$H(s) = \frac{\omega_0}{s + \omega_0}. \tag{2.36}$$

Chapter 3

Simulation and experimental results

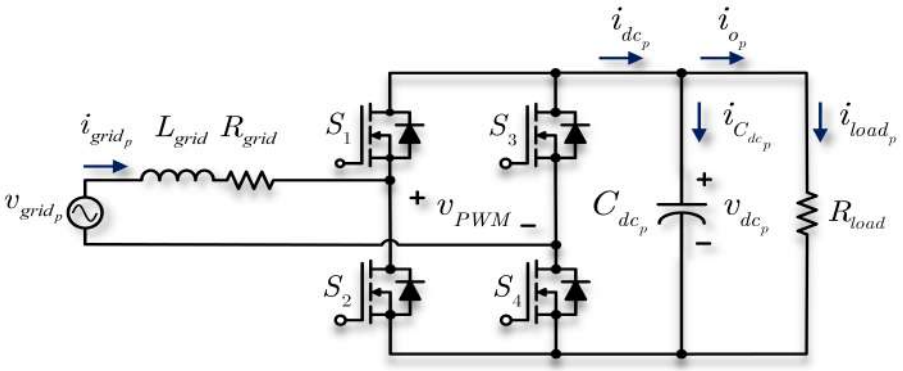
In this chapter, a review of the simulation and the experimental results for both evaluated converters is carried out. In the simulation results, an open-loop scenario under nominal conditions is addressed. Thereafter, a closed-loop scenario is proposed under some disturbances of interest, and some performance parameters are analyzed. Finally, in the experimental results, both converters are studied under open-loop scenarios and their operating principle is validated.

3.1. Bidirectional Buck-Boost converter

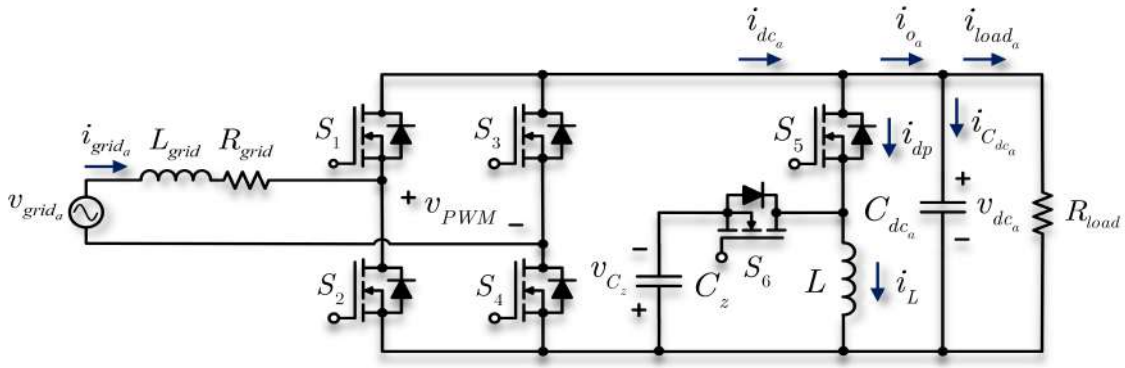
3.1.1. Open-loop simulation of an active front-end rectifier with passive and active power decoupling

This simulation scenario aims to emulate the behavior of a passive decoupling scheme based on the electrolytic capacitor through the active decoupling scheme based on the Bidirectional Buck-Boost converter. In order to validate this scenario, the simulation schemes shown in Fig. 3.1 are proposed.

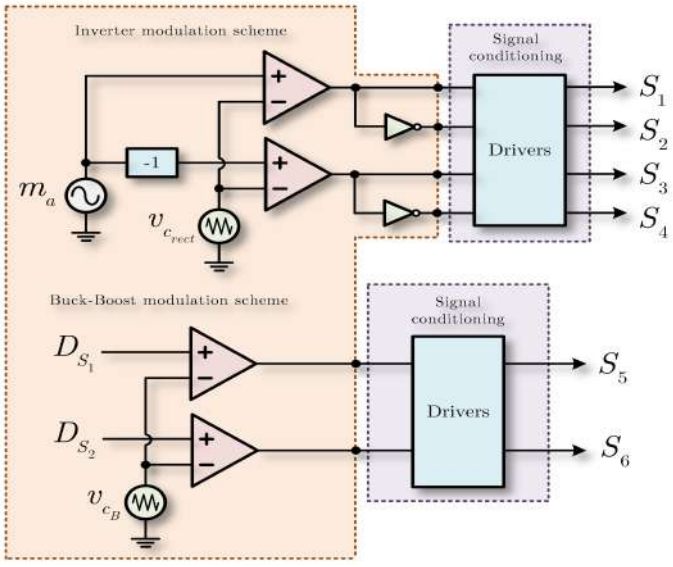
The scheme consists of a single-phase Voltage Source Converter (VSC) which operates as an active front-end rectifier that forms a DC-link, in which the power ripple is presented when it starts supplying power to the load. It is important to remark that a VSC can operate both as a controlled rectifier and as a Full-Bridge inverter and in both cases, the power ripple phenomenon is still present. The decoupling schemes evaluated are a passive scheme (Fig. 3.1-(a)), composed of an electrolytic capacitor, and the active scheme based on the bidirectional Buck-Boost converter (Fig. 3.1-(b)). The modulation schemes for both



(a) VSC with passive power decoupling scheme.



(b) VSC with active power decoupling scheme.



(c) Modulations schemes.

Figure 3.1. Simulation scenarios for the active front-end rectifier with passive and active power decoupling.

converters are shown in Fig. 3.1-(c). Simulation parameters are shown in Table 3.1; these parameters were obtained from the converter sizing in Chapter I.

Table 3.1. Simulation parameters for the active front-end rectifier with passive and active power decoupling.

Parameter	**Symbol**	**Value**	**Unit**
Grid voltage	V_{grid_p}, V_{grid_a}	48	V_{rms}
DC-link voltage	V_{dc_p}, V_{dc_a}	100	V_{avg}
Voltage ripple on the DC-link	ΔV_{dc_p}, ΔV_{dc_a}	10	V_{pp}
Rated power	P_p, P_a	200	W
Grid resistance	R_{grid}	0.4	Ω
Grid inductance	L_{grid}	5.5	mH
Load resistance	R_{load}	50	Ω
Link capacitor for passive decoupling	C_{dc_p}	640	μF
Link capacitor for active decoupling	C_{dc_a}	100	μF
Decoupling capacitor (active scheme)	C_z	100	μF
Transfer inductor	L	620	μH
Switching frequency of VSC	$f_{s_{VSC}}$	10	kHz
Switching frequency of Buck-Boost converter	$f_{s_{APD}}$	50	kHz

In both cases, the load resistance R_{load} is the same in order to supply the same active power of $200W$. The DC-link capacitor for the passive decoupling scheme (C_{dc_p}) is sized to operate under an average voltage level of $100V$ for a voltage ripple of $\Delta V_{dc_p} = 10V_{pp}$. The value of this capacitor should be approximately $640\mu F$. On the other hand, for the active decoupling scheme, a $100\mu F$ decoupling capacitor is used. In this scheme, the capacitor C_{dc_a} only fulfills the function of minimizing the high-frequency switching components that can be presented in v_{dc_a}. The great advantage of the active decoupling scheme over the passive decoupling scheme is that the required DC-link capacitance can be reduced so that it is no longer essential to use electrolytic capacitors and film capacitors can be used instead.

The first graph of Fig. 3.2 shows the simulation corresponding to scenarios (a) and (b) of Fig. 3.1. In the first instance, the voltage and current supplied by the electrical grid for the scheme based on passive power decoupling are shown respectively (v_{grid_p} and i_{grid_p}). Then v_{grid_a} and i_{grid_a} represent the voltage and current supplied by the grid for the active decoupling scheme. It is important to highlight that the voltages v_{grid_p} and v_{grid_a} are practically overlapped and no difference is found between them since the magnitudes for both the passive and the active decoupling schemes tend to be identical, since the same power conditions are considered for both schemes.

The second graph of Fig. 3.2 shows the active power supplied to the load R_{load}, which corresponds to the approximate value of $210W$. A power of $200W$ is initially expected,

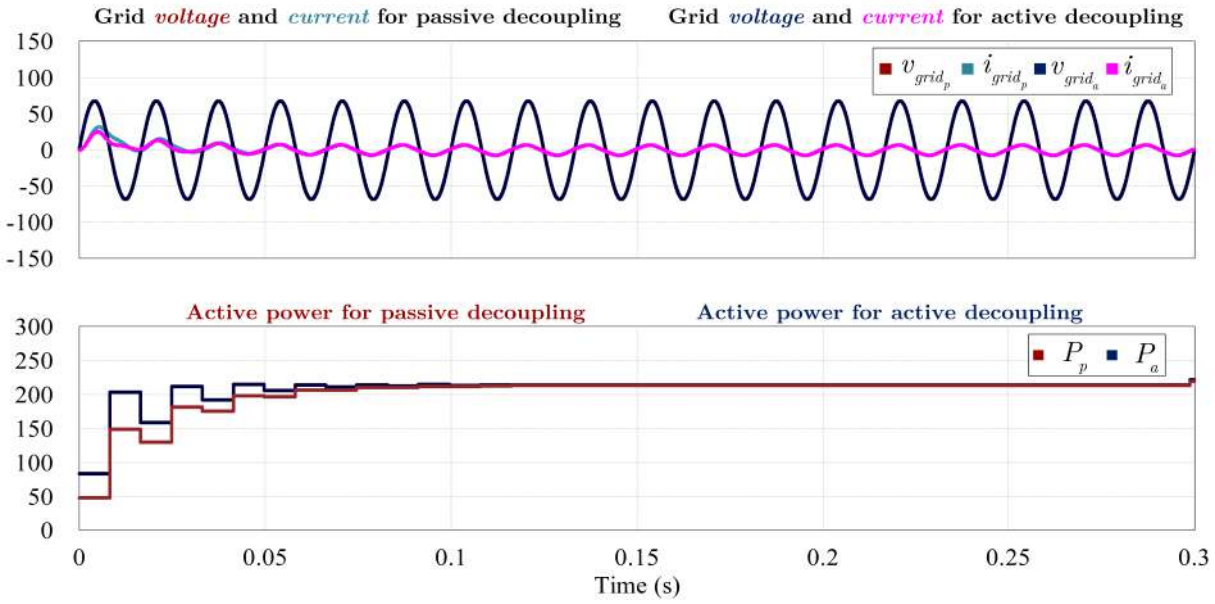


Figure 3.2. Grid voltages and currents and active power for both passive and active decoupling schemes.

however, this variation is justified because of the error in steady state in the DC-link voltage due to the absence of the controller. However, it can be seen for both passive and active decoupling schemes, the active power tends to converge to the same value in steady-state since the operating conditions for both schemes are the same.

The Fig. 3.3 shows the instantaneous and average voltage on the DC-link for both passive and active decoupling schemes (v_{dc_p}, V_{dc_p} and v_{dc_a}, V_{dc_a}). It can be seen from the latter that the average value reaches approximately $100V$ and the ripple voltage ranges in $10V_{pp}$ for both cases. In addition, it can be highlighted that the average voltage in the active decoupling scheme has a faster response than in the passive decoupling scheme; this is mainly because the value of the capacitance C_{dc_a} is at least six times lower than C_{dc_p}, therefore the dynamic response offered by the active scheme is much faster. It can also be remarked on the presence of the second harmonic at $2\omega_0$.

In Fig. 3.4 the instantaneous and average voltages on the decoupling capacitor C_z are shown. It can be seen that the average voltage reaches an approximate value of $180V$ and the ripple voltage ranges in $30V_{pp}$. It should be noted that the capacitor C_z must withstand large voltage oscillations and thus the ripple voltage on the DC-link is reduced. The operating principle consists of diverting the ripple energy that is present in v_{dc_a} towards the capacitor C_z. As shown in Chapter I, the Bidirectional Buck-Boost converter allows adjusting of the voltage on the decoupling capacitor in order to regulate the magnitude of the ripple on v_{dc_a}, so that the voltage v_{C_z} can either increase or decrease depending on the parameters required on v_{dc_a} and the control objectives.

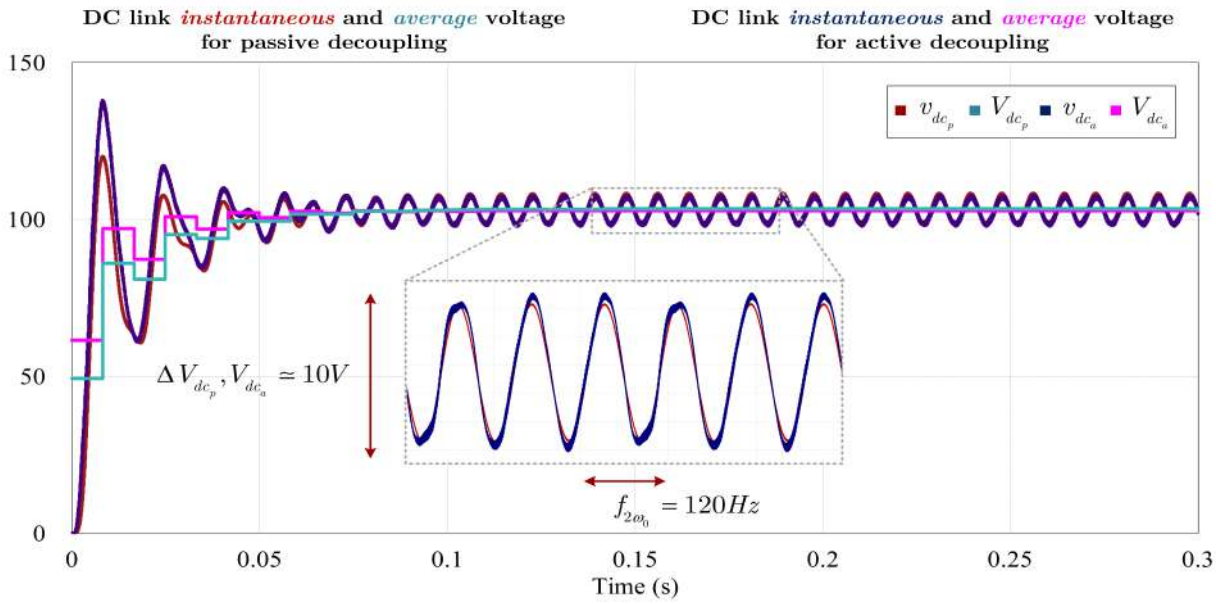


Figure 3.3. Instantaneous and average voltages on the DC-link capacitor for both passive and active schemes.

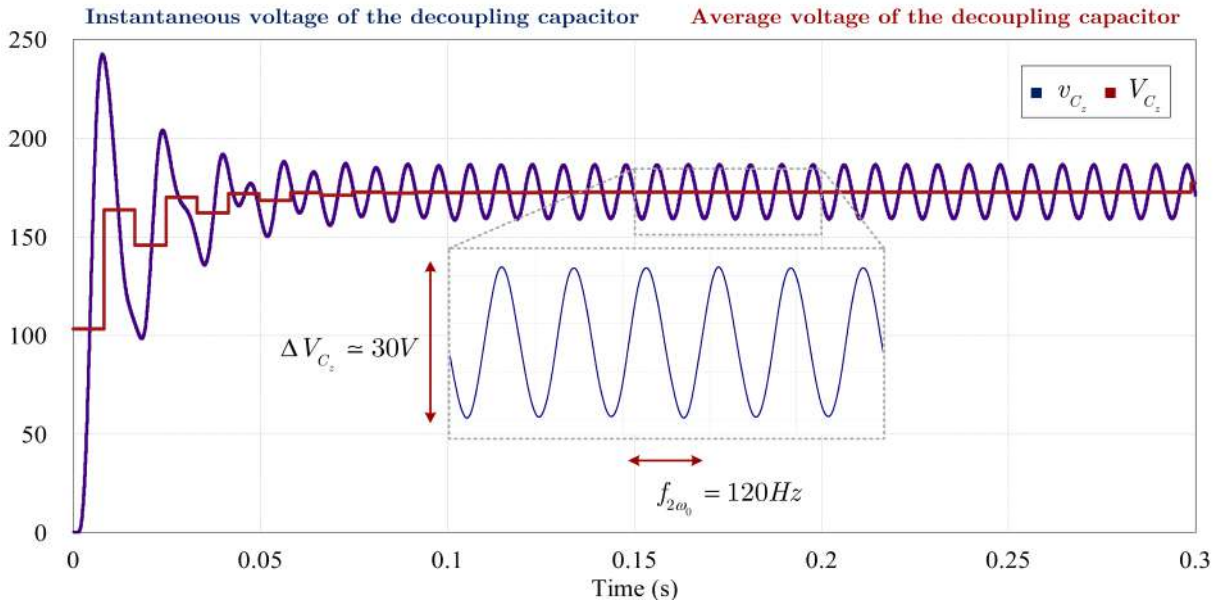


Figure 3.4. Instantaneous and average voltages on the decoupling capacitor.

Fig. 3.5 shows the drain-source voltage on S_1 and the sum of the decoupling capacitor voltage and the DC-link voltage; i.e., $v_{C_z} + v_{dc_a}$. It can be seen that when S_1 is off, the drain-source voltage is equal to the sum of the decoupling capacitor and the DC-link voltages; that is:

$$V_{S_{1_{max}}} = V_{C_{z_{max}}} + V_{dc_{a_{max}}}. \tag{3.1}$$

From Eq. 3.1, the maximum allowable voltage for the power switch can be defined;

the sizing procedure is specified in Chapter I, section 1.5. For this simulation scenario, a drain-source voltage level of no higher than $300V$ was considered. This must be taken into account when sizing since the DC-link ripple is limited by how much the decoupling capacitor voltage level can be boosted and therefore under what voltage level the switch can operate. It should be remarked that there is a slope on the switch voltage during the falling edge due to the integration step, however, the results are still legit.

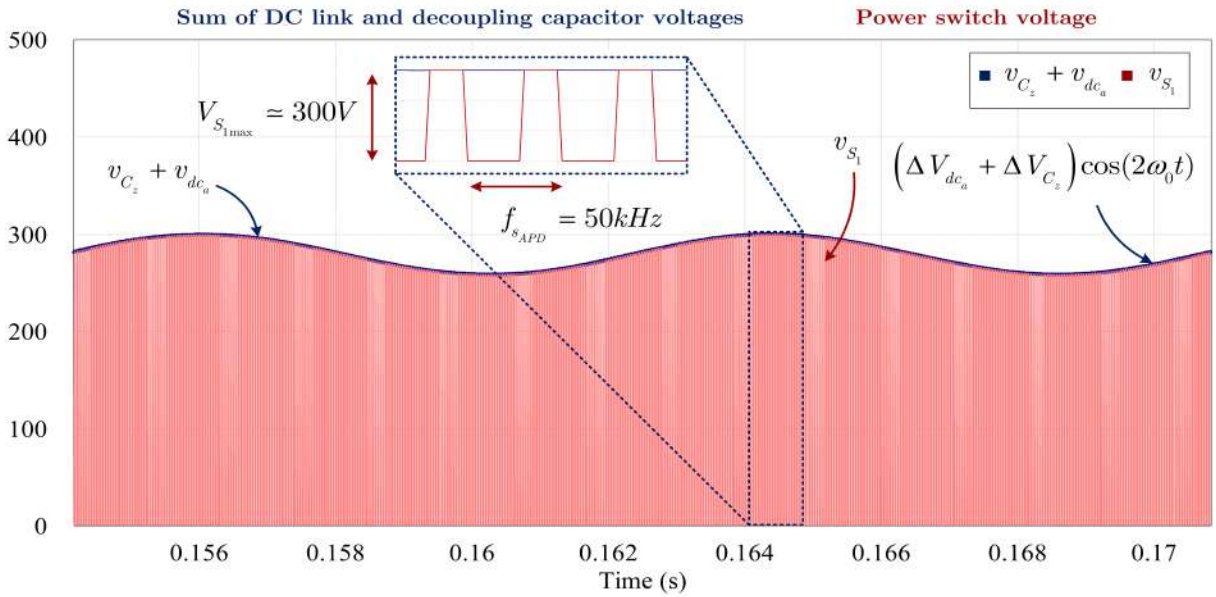


Figure 3.5. Power switch voltage.

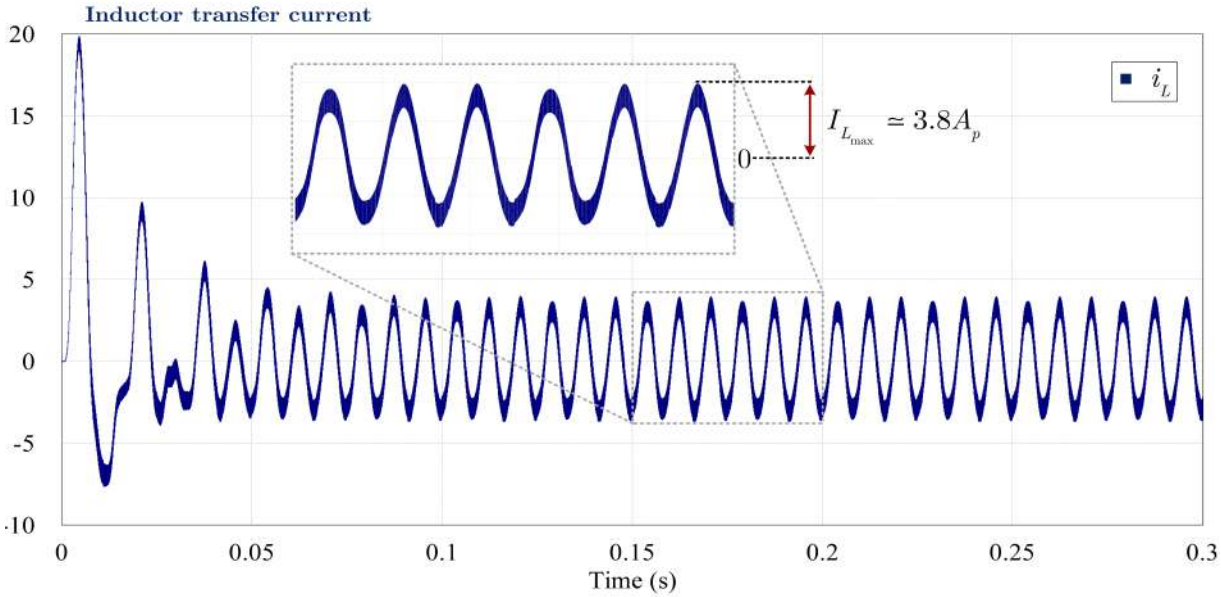


Figure 3.6. Instantaneous current across the transfer inductor.

Fig. 3.6 shows the current across the transfer inductor L of the Bidirectional Buck-Boost converter. It can be noted that the inductor operates in DCM since the current is less than zero in each negative half cycle. This behavior is normal and expected in this converter since in the negative half cycle the capacitor releases the energy toward the DC-link and this causes the current across the inductor to be negative. It can also be highlighted that the maximum value of the current in steady-state does not exceed $5A$, which corresponds to the dimensioning carried out in chapter I.

3.1.2. Closed-loop simulation of active front-end rectifier with passive and active power decoupling

This simulation scenario aims to validate the operation of the proposed control system and compare the performance of the active decoupling scheme against the passive decoupling scheme facing load changes. The simulation and the control schemes are shown in Figs. 3.7 while the simulation parameters are the same addressed in Table 3.1.

The control objective for the passive decoupling scheme is to regulate the average voltage on the DC-link in response to load variations through the active front-end rectifier. For this control scheme, a cascade-loop control is used to regulate the voltage level on the DC-link [47, 48]; the cascade-loop controller is not analyzed in depth in this work, since it is only used for performing comparisons between the passive and active decoupling schemes. In the case of the active decoupling scheme, the control objective is to regulate the average value of the voltage on the decoupling capacitor C_z and transfer the ripple voltage from C_{dc_a} to C_z. The voltage reference for v_{C_z} can be obtained at first from the desired ripple voltage on the DC-link. However, the maximum permissible voltage on the power switches can also be a restriction for implementation.

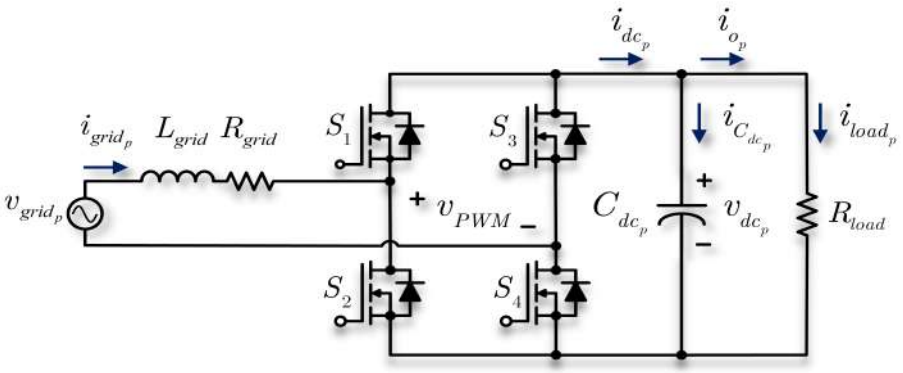
It is important to highlight that the cascade-loop control is decoupled from the active power decoupling control since the bandwidths of both are separated enough for at least one decade. The simulation sequence is explained below (view Fig. 3.8):

1. From 0 to $t_1 = 0.15s$ a purely resistive load of $R_L = 50\Omega$ is connected for supplying $200W$.

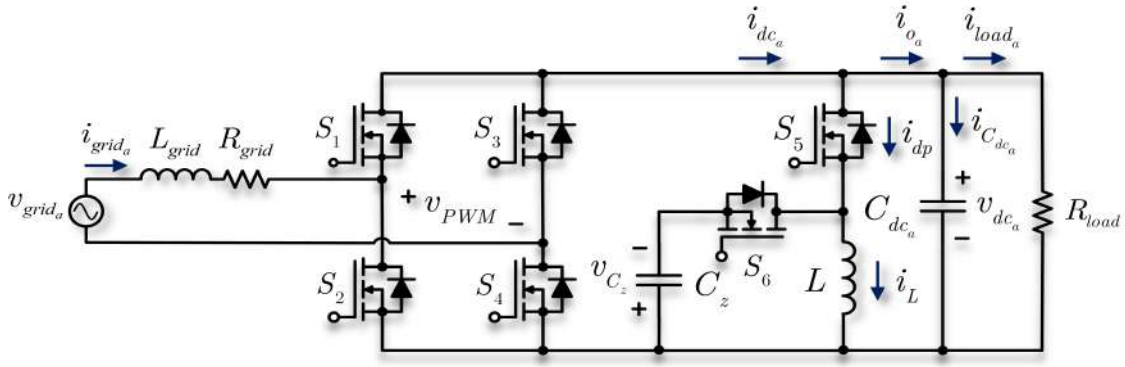
2. From $t_1 = 0.15s$ to $t_2 = 0.3s$, the load is halved in order to supply $400W$.

3. Finally, since $t_2 = 0.3s$, the load is set to $R_L = 100\Omega$ for supplying $100W$.

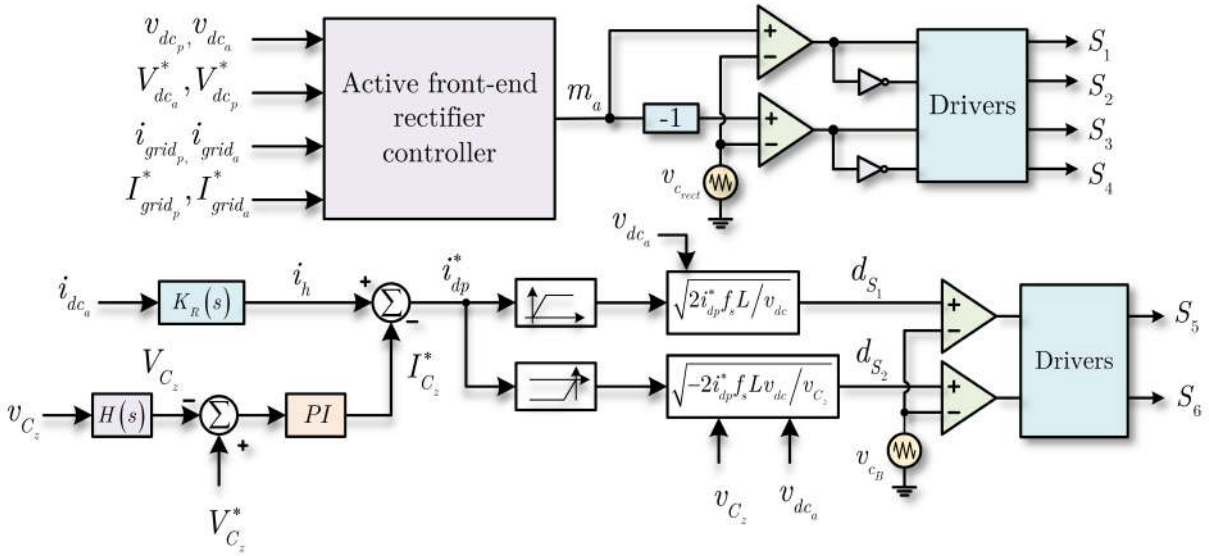
Fig. 3.9 shows the DC-link voltage for both passive and active schemes. It can be observed that the average value remains regulated at $100V$ as expected. However, the



(a) VSC with passive power decoupling scheme.



(b) VSC with active power decoupling scheme.



(c) Control and modulations schemes.

Figure 3.7. Closed-loop simulation scenarios for the active front-end rectifier with passive and active power decoupling.

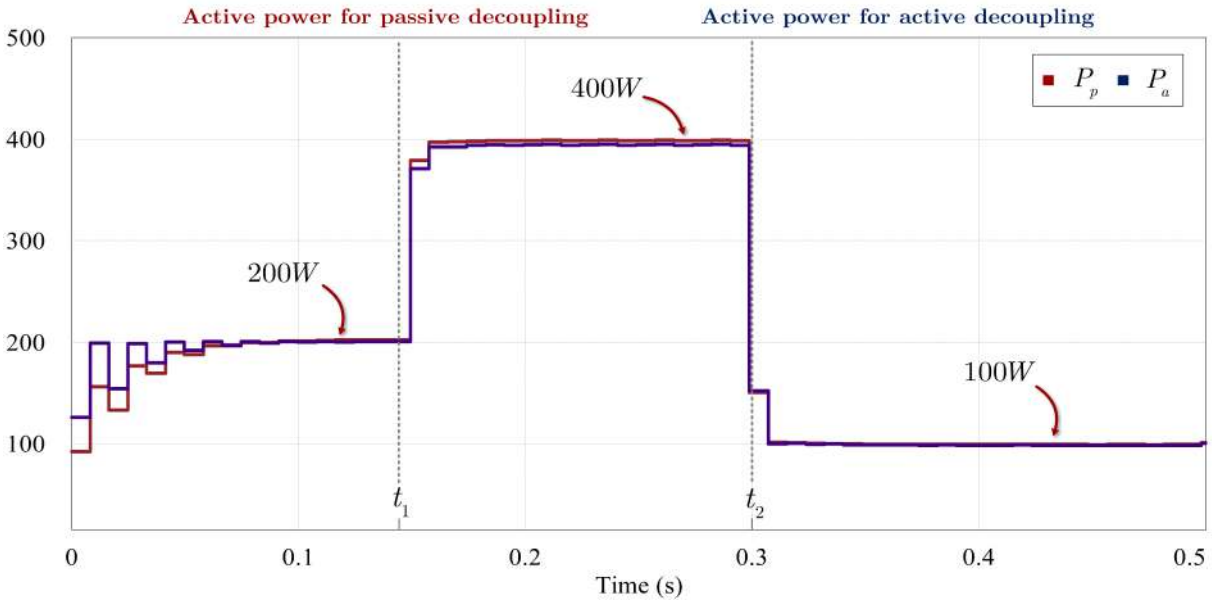


Figure 3.8. Active power sequence.

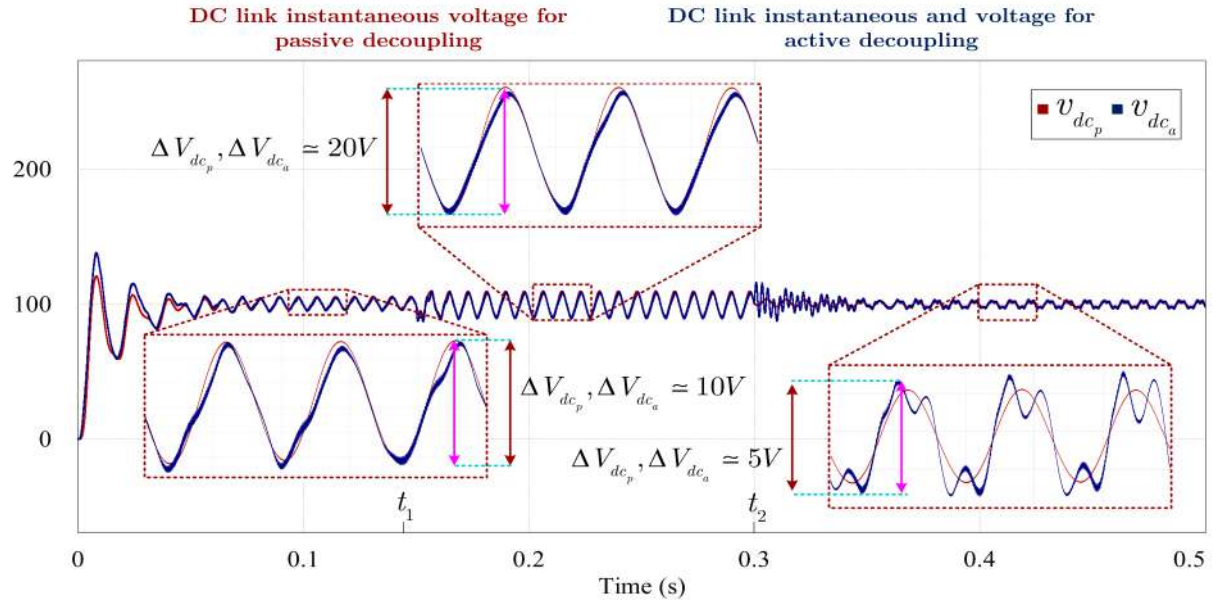


Figure 3.9. DC-link voltages for passive and active decoupling schemes.

ripple voltage changes at t_1 from $10V$ to $20V$ and from $20V$ to $5V$ at t_2. This phenomenon is expected since in the passive decoupling scheme, the active front-end rectifier is only in charge of regulating the average value of the DC-link and, being constant, the value of the voltage ripple relies directly on the value of the capacitor C_{dc_p} and the power supplied to the load. In the active decoupling scheme, the rectifier is also responsible for regulating the average value on the DC-link, however, the Bidirectional Buck-Boost converter performs the task of reducing the ripple in v_{dc_a}. The active decoupling scheme control system can

either regulate the voltage at C_z and allow different oscillations at v_{dc_a} or maintain a constant ripple level at v_{dc_a} at the rate of allowing the voltage in C_z to vary. For this scenario, the voltage in C_z is regulated and different oscillations are allowed in v_{dc_a} in order to limit the maximum stress voltage on the power switches.

Fig. 3.10 shows the voltage reference ($V_{C_z}^*$) on the decoupling capacitor, the average voltage (V_{C_z}) and the instantaneous voltage (v_{C_z}). It can be seen that the average value follows the reference of $180V$ regardless of load changes. It can also be highlighted that there is a linear relationship between the DC-link ripple voltage and the decoupling capacitor ripple voltage; that is, they both change in the same proportion. This must be taken into account when defining voltage limits. It must be noted that the controller works properly because the maximum error corresponds when $V_{C_z} = 178.5V$ which implies a deviation of approximately 0.85%.

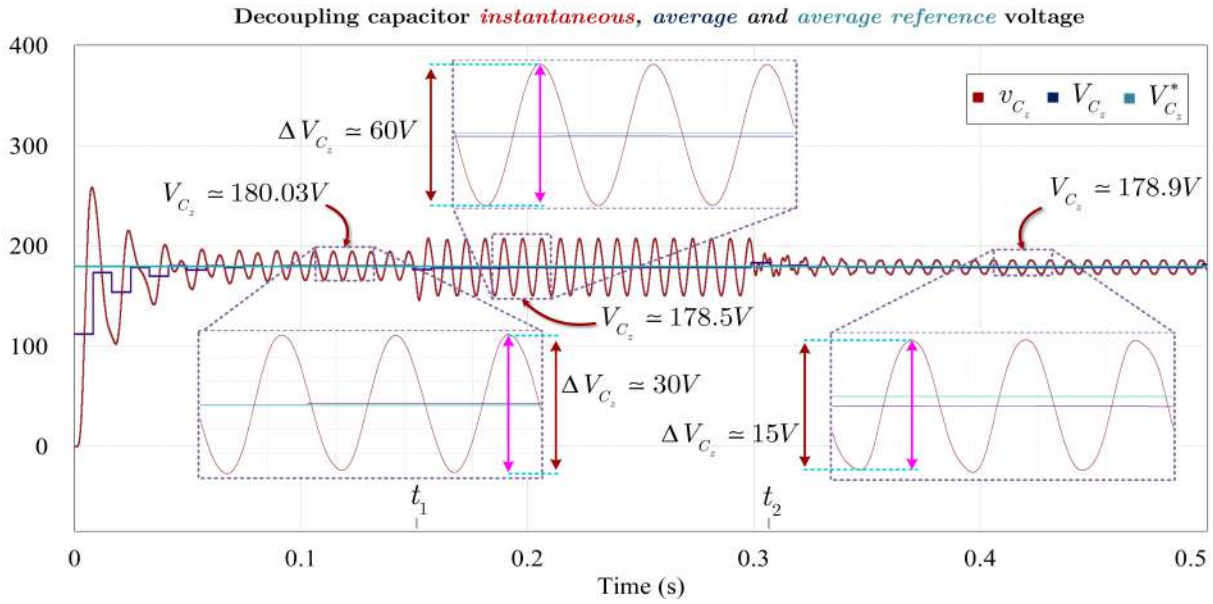


Figure 3.10. Reference and actual value of the decoupling capacitor voltage.

The first graph in Fig. 3.11 shows the current provided by the active front-end rectifier (i_{dc_a}) and the current flowing through the Bidirectional Buck-Boost converter stage (i_{dp}). It can be distinguished that the harmonic i_h at $2\omega_0$ is deflected through the active decoupling stage; that is, $i_h = i_{dp}$. This produces that in the output current i_{load_a} only the average value is manifested as shown in the second graph in Fig. 3.11.

In Fig. 3.12 the frequency spectrum since $t = 0.4d$ of the signals in Fig. 3.11 is shown, however, similar behaviors of the frequency spectrums for all time intervals in steady-state are expected. In the first graph, it can be confirmed that $i_h = i_{dp}$ since the current i_{dp} has the same harmonic content as i_{dc_a} being the average component the exception. The

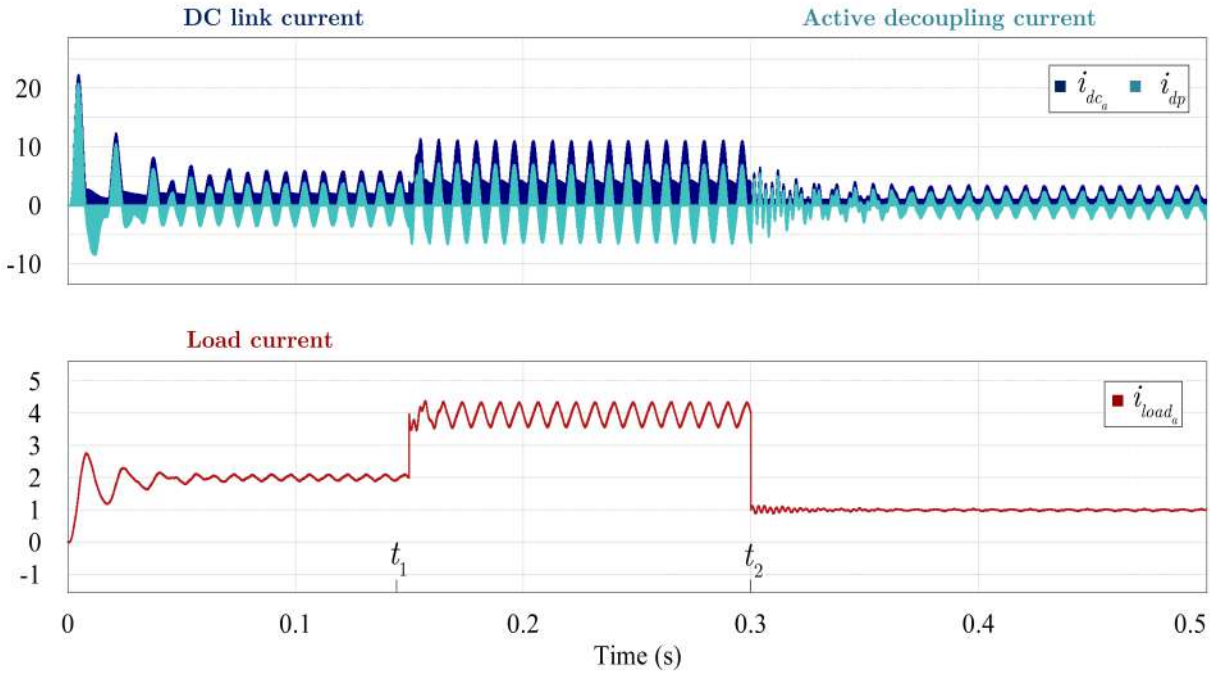


Figure 3.11. Current provided by the front-end rectifier (i_{dc_a}). Current diverted by the active decoupling stage (i_h). Load current (i_{load_a}) for the active decoupling scheme.

second graph in Fig. 3.12 shows that the load current i_{load_a} is mostly made up of the average component and the high-order harmonics are mitigated.

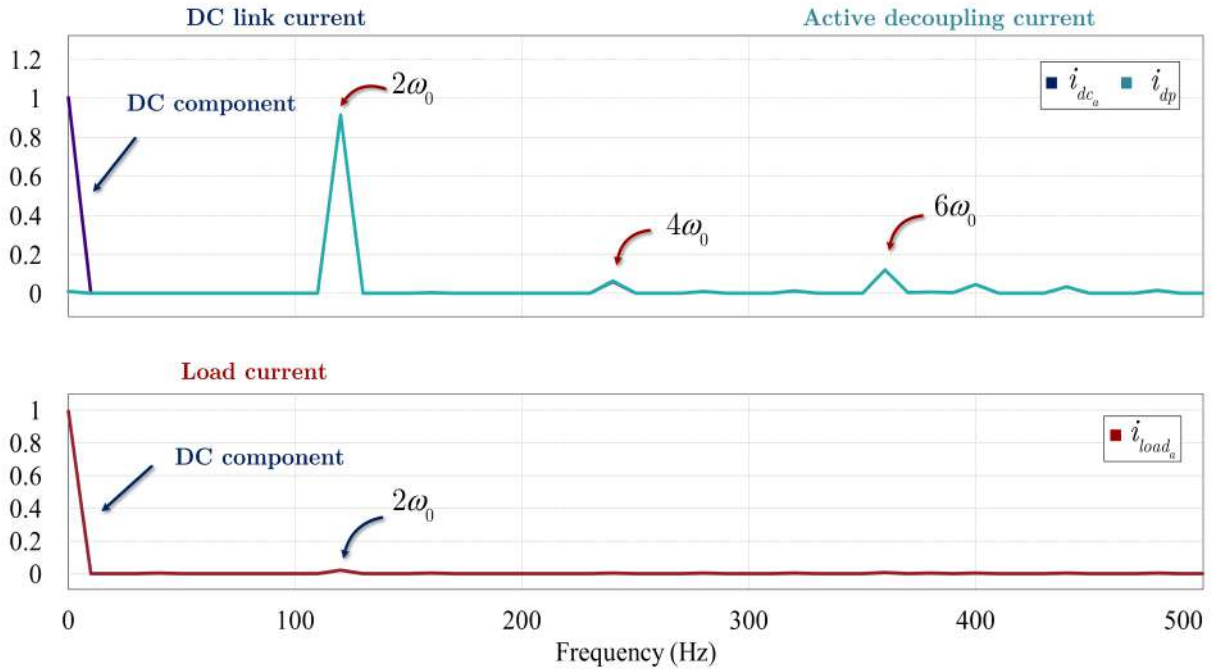
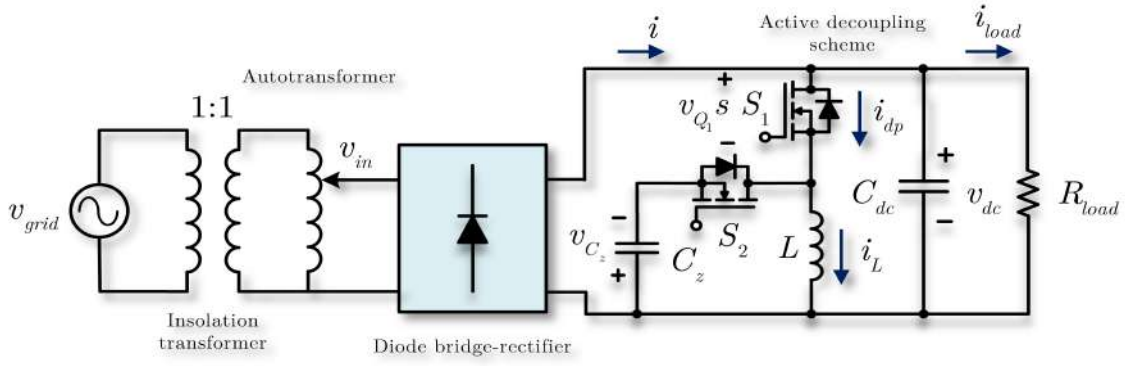


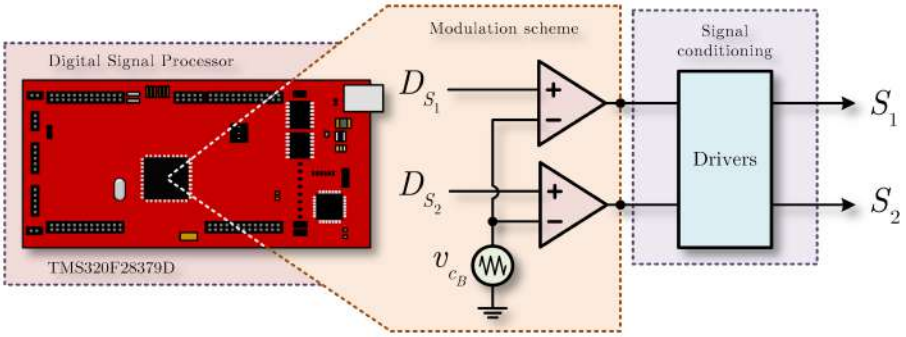
Figure 3.12. Frequency spectrum for the currents shown in Fig. 3.11.

3.1.3. Experimental scenario for a Full-bridge diode rectifier with active power decoupling

This experimental scenario aims to validate the operation principle of the Bidirectional Buck-Boost converter as an active power decoupling scheme in open-loop scenarios. It is important to remark that despite the experimental scenarios differ from the simulation scenarios, these are still legitimate and valid since independently of which scheme is used either the VSC as rectifier/inverter or the diode full-bridge rectifier, the power ripple at $2\omega_0$ is present anyway and the magnitude of this ripple power relies on the supplied power and not on the scheme type. The change from the simulation to the experimental scenarios was performed for reasons of practicality and simplicity; furthermore, other experimental scenarios that complement the overall results are presented below, allowing diversifying the outcomes by testing the power converter in multiple conversion schemes.



(a) Full-bridge diode rectifier with active power decoupling based on the Bidirectional Buck-Boost converter.



(b) Modulation scheme for the experimental scenario.

Figure 3.13. Experimental scenario and modulation schemes for the Full-bridge diode rectifier with active power decoupling based on the Bidirectional Buck-Boost converter.

Fig. 3.13 shows the scheme to be evaluated. In the first instance, there is an isolation

transformer that fulfills the task of isolating the electrical grid from the power circuit. Afterward, there is an autotransformer that meets the task of regulating the AC voltage at the input of the single-phase diode bridge rectifier; this way, the voltage level on the DC-link can be boosted gradually. Subsequently, there is the active decoupling scheme based on the Bidirectional Buck-Boost converter; this converter is responsible for reducing the ripple voltage present on the DC-link. The capacitor C_{dc} only fulfills the task of reducing the high-frequency switching components. Finally, a purely resistive load of 50Ω is used as an output load. An experimental scenario of $50W$ is first performed and then the rated power scenario of $200W$ is addressed. For the modulation scheme, a Digital Signal Processor (TMS320F28379D) from Texas Instruments is used for controlling the power transistors. The experimental parameters are shown in Table 3.2; these parameters are raised on the converter sizing addressed in Chapter I, section 1.5.

Fig. 3.14 shows the built experimental test bench for the scheme raised in Fig. 3.13.

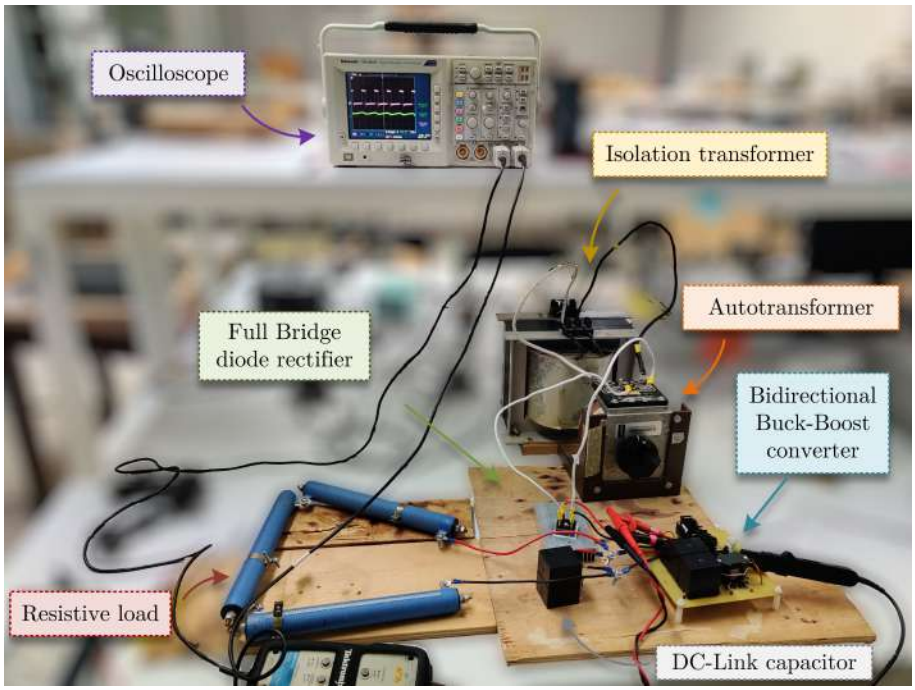


Figure 3.14. Experimental test bench.

Fig. 3.15 shows in channels 3 and 4 the voltage on the DC-link and the current across the transfer inductor respectively when the converter operates with no load connected. It can be seen that the voltage ripple is null, however, a high-frequency induced noise appears because of the MOSFET switching at $50kHz$. The transfer inductor current swings around zero.

Channels 3 and 4 of Fig. 3.16 show the DC-link voltage (v_{dc}) and output current(i_{load}) respectively when $R_{load} = 50\Omega$ is connected. At this point, it can be seen how the

Table 3.2. Experimental parameters for the Full-bridge diode rectifier with active power decoupling.

Parameter	**Symbol**	**Value**	**Unit**
DC-link voltage	V_{dc}	50, 100	V_{avg}
Rated power	P_o	200	W
Testing power	P_o	50	W
Load resistance	R_{load}	50	Ω
Link capacitor	C_{dc}	100	μF
Decoupling capacitor	C_z	100	μF
Transfer inductor	L	620	μH
Switching frequency of Buck-Boost converter	$f_{s_{APD}}$	50	kHz

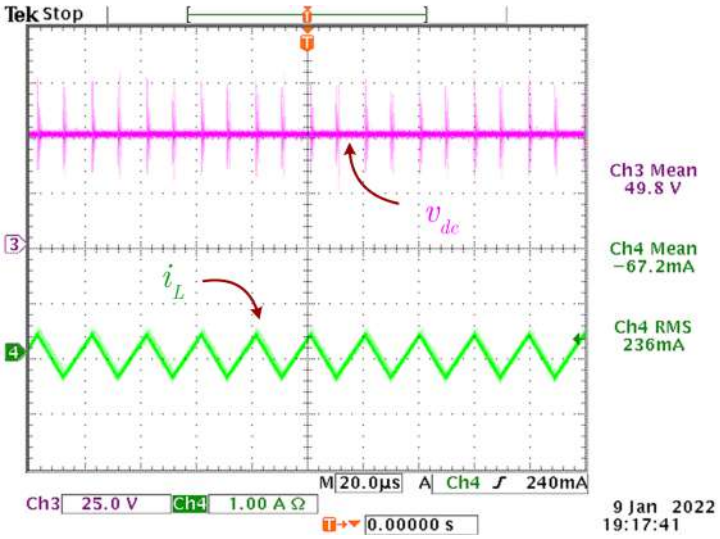


Figure 3.15. DC-link voltage and transfer inductor current operating with no load connected.

voltage ripple at the terminals of C_{dc} shows up and how the Bidirectional Buck-Boost converter performs the task of attenuating and buffering the ripple voltage, keeping it at an approximate value of $12V_{pp}$.

Channel 3 of Fig. 3.17 shows the voltage across the decoupling capacitor C_z. Here it can be distinguished that it withstands larger oscillations than that of the DC-link voltage since it swings with a ripple voltage of approximately $21V_{pp}$. This is an expected phenomenon since in order to reduce the ripple voltage on the DC-link it is necessary to allow large fluctuations in the voltage level of the decoupling capacitor. Considering the average and the ripple voltage and the capacitance value of both decoupling and DC-link capacitors, it can be concluded that the ripple voltage on the DC-link is reduced approximately 5.2 times, which is the expected value from the analysis carried out in Chapter I.

Finally, Fig. 3.18 channel 3 shows the drain-source voltage on switch S_1. It can be seen that the maximum value of the voltage level when S_1 is off is given by $v_{dc_a} + v_{c_z}$, then

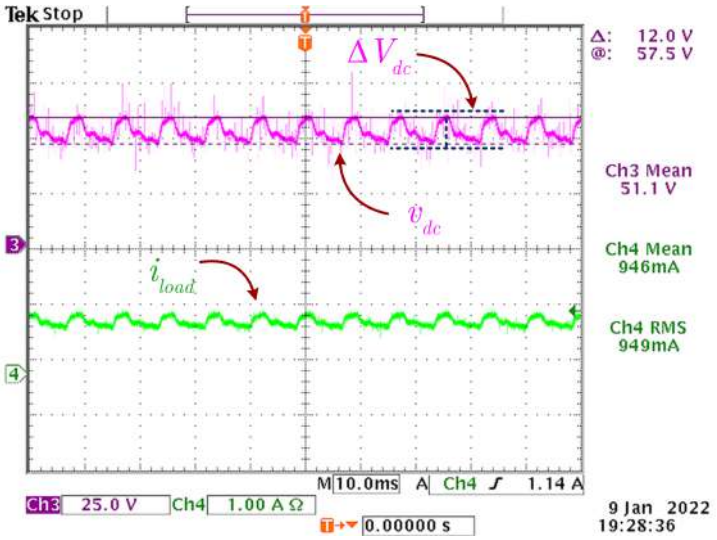


Figure 3.16. DC-link voltage and load current when $R_{load} = 50\Omega$ is connected.

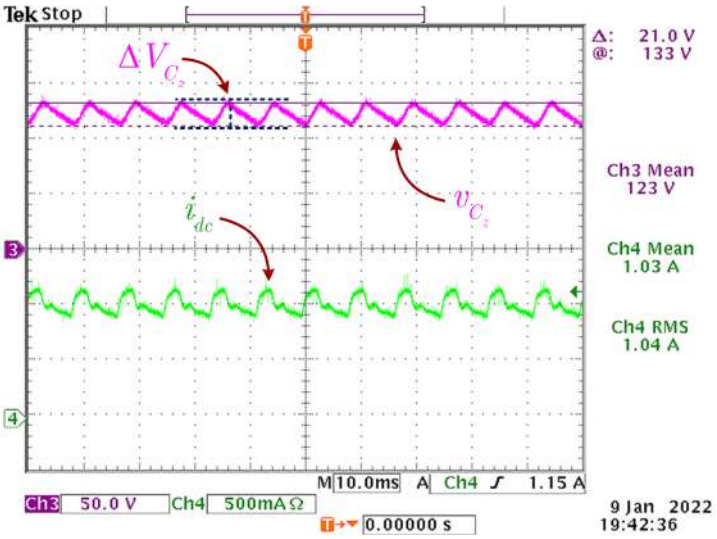


Figure 3.17. Decoupling capacitor and DC-link voltages for a load of $R_{load} = 50\Omega$.

the harmonic at $2\omega_0$ is also present on the switch voltage. It is important to consider the maximum oscillation possible when performing the power switch sizing. Channel 4 shows the current across the transfer inductor L, in which it can be highlighted that it operates in DCM as expected.

Fig. 3.19 shows the experimental results at the rated power of the scheme proposed in Fig. 3.13. Channel 1 shows the DC-link voltage where it can be seen that the Bidirectional Buck-Boost converter operates properly, being able to reduce the voltage ripple present on the DC-link to a value of approximately $36V$. The converter at this point operates in open-loop and at a duty cycle of 80%; this implies that the voltage ripple could be reduced to an even greater extent, however, for safety reasons, it was limited to 80% due

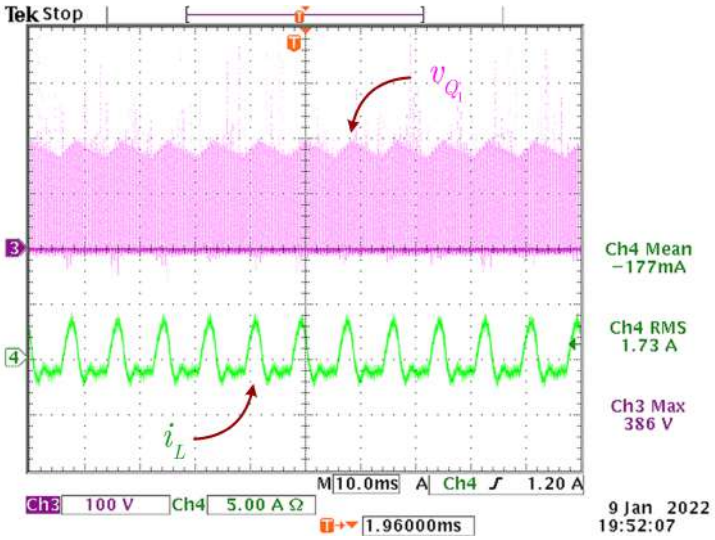


Figure 3.18. Drain-source voltage for switch S_1 and transfer inductor current for a load of $R_{load} = 50\Omega$.

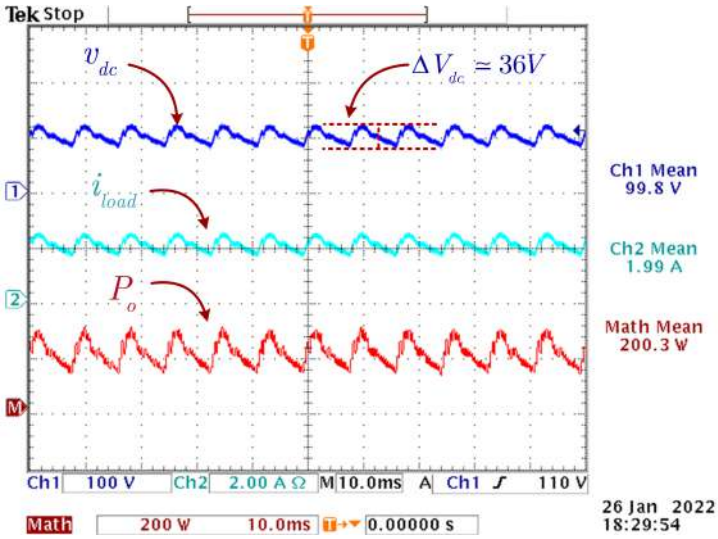


Figure 3.19. Experimental results for the rated power scenario of $200W$. *Ch1* represents the DC-link voltage. *Ch2* shows the current demanded by the resistive load. *Ch3* shows the instantaneous active power dissipated by the load.

to some problems with radiated noise since this represents a risk because it compromises the converter's operation. Channel 2 shows the current demanded by the resistive load and channel 3 shows the active power it dissipates.

3.1.4. Experimental scenario for a DC/AC single-phase inverter with passive and active power decoupling

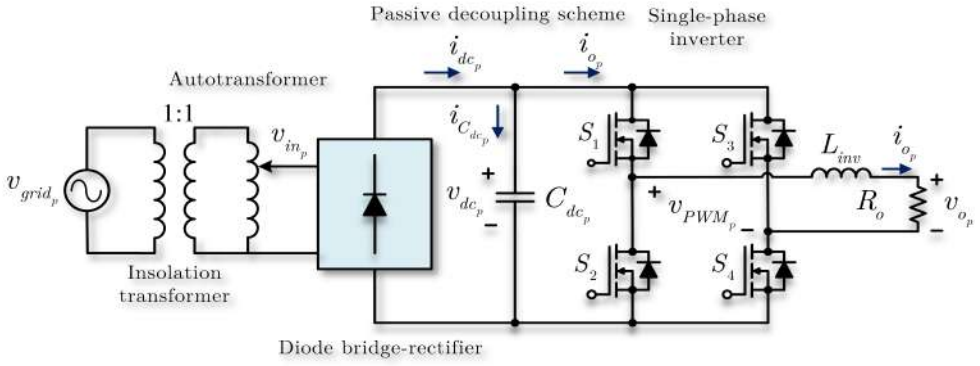
This experimental scenario aims to operate and compare the passive and active decoupling schemes interconnected to a Full-Bridge single-phase inverter for supplying active power

to a purely resistive load at the output. Fig. 3.20 shows the scheme to be evaluated, which also consists of a full-wave diode single-phase rectifier bridge that forms the DC-link voltage at the inverter's input. Afterward, an electrolytic capacitor is used as the passive decoupling scheme (view 3.20-(a)). A Full-Bridge single-phase DC/AC converter is incorporated to supply active power to the load. In the second scenario (view Fig. 3.20-(b)), nearly the same previous scheme is shown, but now the Bidirectional Buck-Boost converter is used as the active decoupling scheme. Fig. 3.20-(c) shows the modulation schemes for both experimental scenarios. The experimental parameters are shown in Table 3.3. It is important to highlight that this scenario was raised because of the voltage overshoots present on the power switches, then a testing power of $50W$ was redefined. Given this experimental scenario, the converter parameters do not have to change since it is dimensioned for a power of $200W$.

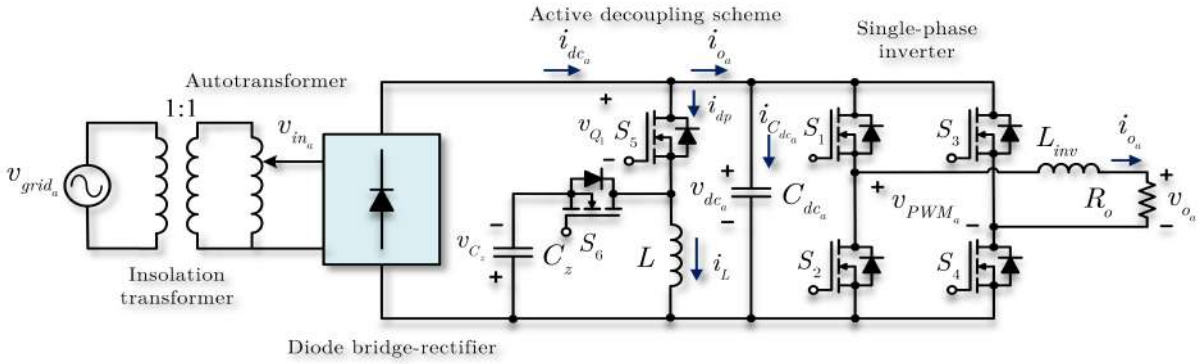
Table 3.3. Experimental parameters for the DC/AC single-phase inverter with passive and active power decoupling.

Parameter	**Symbol**	**Value**	**Unit**
Output voltage	V_{o_p}, V_{o_a}	48	V_{rms}
DC-link voltage	V_{dc_p}, V_{dc_a}	50	V_{avg}
Voltage ripple on the DC-link	ΔV_{dc_p}, ΔV_{dc_a}	10	V_{pp}
Testing power	P_p, P_a	50	W
Inverter filter's inductor	L_{inv}	600	μF
Load resistance	R_o	16	Ω
Link capacitor for passive decoupling	C_{dc_p}	1,100	μF
Link capacitor for active decoupling	C_{dc_a}	100	μF
Decoupling capacitor (active scheme)	C_z	100	μF
Transfer inductor	L	620	μH
Switching frequency of Full bridge inverter	$f_{s_{VSC}}$	10	kHz
Switching frequency of Buck-Boost converter	$f_{s_{APD}}$	50	kHz

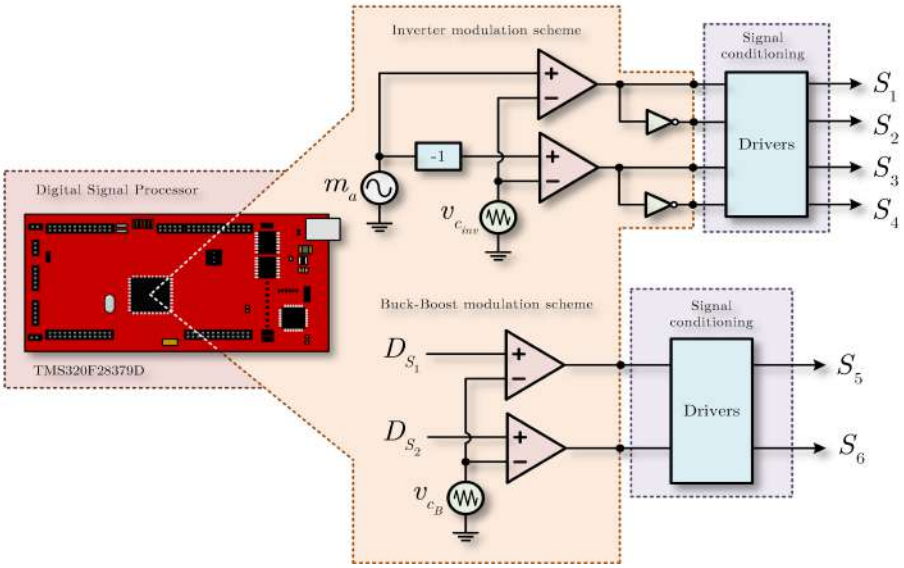
Initially, it was contemplated to operate the converter at the nominal power of $200W$ under which it was previously designed, however, due to voltage overshoots on the drain-source terminals of the power switches, it was decided to design and adapt a snubber circuit to minimize the effect of voltage overshoots in S_5 and S_5. This is an undesirable phenomenon that is mostly present due to the effects of equivalent parasitic inductances and capacitances in the final circuit. With the incorporation of this snubber circuit, it was necessary to reduce the maximum operating power due to the amount of power that the snubber can dissipate, since if the converter operates at higher power, the power dissipated in the snubber increases and the same way. Even though this implies an important drawback and reduces the overall efficiency of the system, experiments can



(a) DC/AC converter with passive decoupling.



(b) DC/AC converter with active decoupling based on the Bidirectional Buck-Boost converter.



(c) Modulation schemes for both experimental scenarios.

Figure 3.20. Experimental scenarios for the DC/AC single-phase inverter with passive and active power decoupling.

still be carried out to validate the operating principle of the converter and compare both passive and active schemes.

In Fig. 3.21 the results for the passive decoupling scheme are shown. Channels 1 and 3 display the inverter output voltage and the current demanded by the load respectively, supplying a total of $50W$. On channel 2, the DC-link voltage is displayed at an average value of approximately $50V$. The same waveforms are shown in Fig. 3.22, but with the system operating with the Bidirectional Buck-Boost converter as the active decoupling scheme. It can be seen that in the passive decoupling scheme, a ripple level of $11.2V_{pp}$ is reached with a $1,100\mu F$ electrolytic capacitor. On the other hand, in the active decoupling scheme, a ripple level of $12.8V_{pp}$ is reached, however, an equivalent capacitance of $200\mu F$ is used considering C_{dc_a} and C_z; furthermore, the ripple voltage in this last scheme can be further reduced by increasing the duty cycle of the converter. It can be seen that the Voltage Total Harmonic Distortion (THD_v) for both active and passive decoupling schemes is high, however, this is justified because the THD_v parameter was not considered as a performance parameter since this scenario aimed to compare only the ripple voltage attenuation for both schemes; nevertheless, the THD_v can be optimized by designing a proper LC/LCL filter and by reaching a lower ripple voltage on the DC-link.

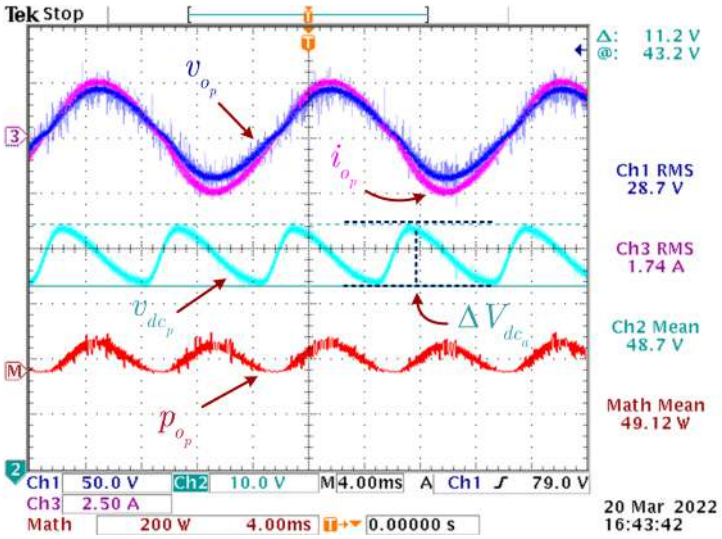


Figure 3.21. Experimental results for the DC/AC converter with passive decoupling.

With these experimental results, it can be concluded that the DC-link capacitance for the power conditions established in the Table 3.3 can be reduced approximately 11 times the initial value of the DC-link capacitor and the total equivalent capacitance can be reduced from $1{,}100\mu F$ to $200\mu F$, which represents a decrease of approximately 81.81% of the initial value when using the Bidirectional Buck-Boost converter as an active decoupling scheme, substituting the passive decoupling scheme. By obtaining this

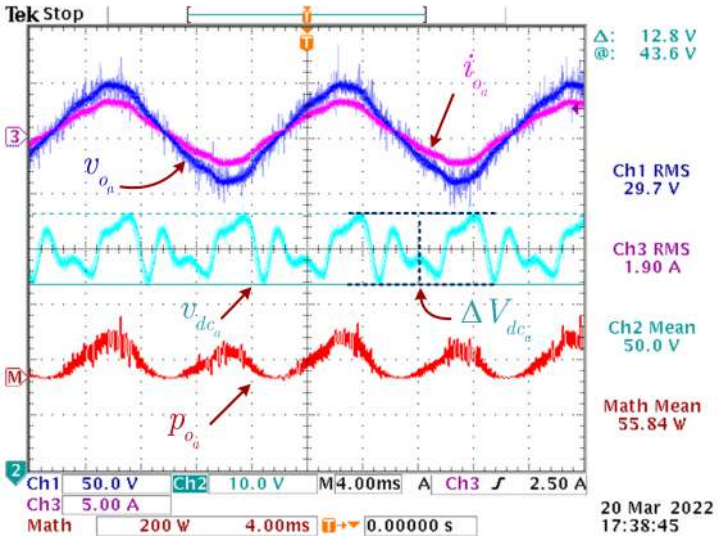


Figure 3.22. Experimental results for the DC/AC converter with active decoupling.

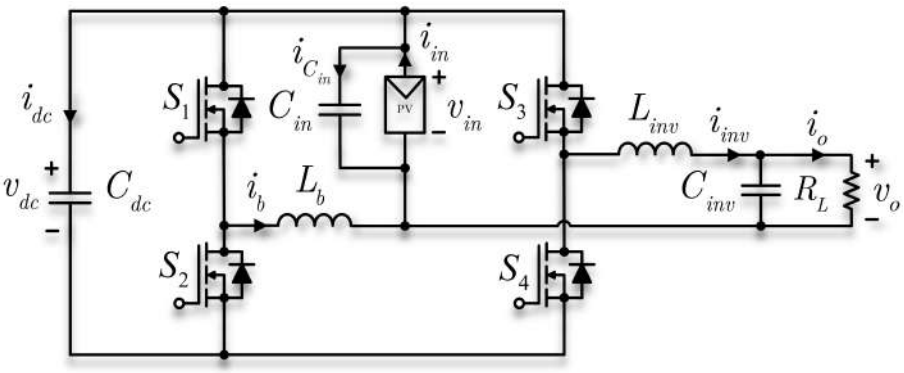
reduction of the total equivalent capacitance, it is possible to replace electrolytic capacitors with film capacitors and improve the performance parameters of the overall system by taking advantage of the benefits of this type of capacitors.

3.2. DC/AC converter with dependent active power decoupling

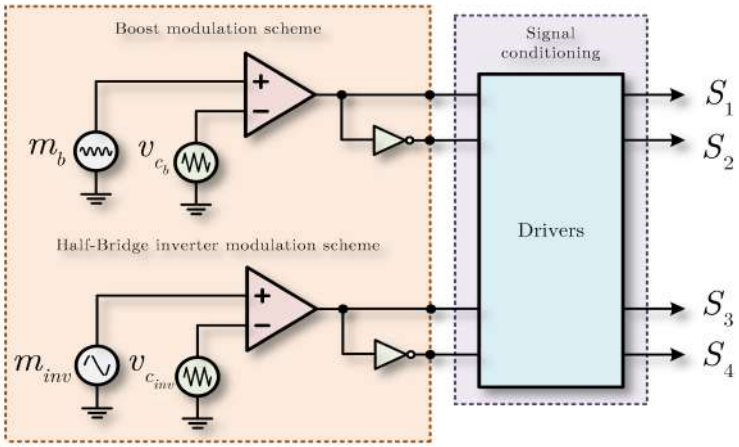
3.2.1. Open-loop simulation for the DC/AC converter with dependent active power decoupling as a forming converter

This simulation scenario aims to validate the operation principle of the DC/AC converter with a dependent active power decoupling feature under nominal conditions in an open-loop simulation. In order to validate this scenario, the simulation scheme shown in Fig. 3.23 is proposed.

The scheme consists of the DC/AC converter with active power decoupling presented in Chapter II. In the first instance, the input power source is a photovoltaic system made up of a series connection of six photovoltaic panels, resulting in an input voltage v_{in} of approximately $205V$. It is also composed of the transfer inductor L_b and the DC-link capacitor C_{dc}. At the Half-Bridge output, there is the LC filter made up of the inductor L_{inv} and the capacitor C_{inv}. Finally, a purely resistive load is used. The operation principle consists of operating the Half-Bridge inverter as a forming converter to generate an AC bus for the resistive load and to be able to provide the active power that it



(a) DC/AC converter scheme with active power decoupling feature operating as a forming converter.



(b) Modulation scheme for the simulation scenario.

Figure 3.23. DC/AC converter with active power decoupling feature operating as a forming converter.

demands. In addition, the objective is also to reduce the voltage ripple at the terminals of the photovoltaic system by diverting it towards the DC-link capacitor. The simulation parameters are shown in Table. 3.4. These parameters are obtained from the converter sizing addressed in Chapter II, section 1.4.

Fig. 3.23 shows that the converter operates adequately for the established nominal conditions. The first graph shows the voltage at the output of the Half-Bridge stage after the LC filter. A measurement of the voltage Total Harmonic Distortion (THD_v) in v_o was carried out and a value of less than 0.52% was obtained. The second graph shows the current demanded by the resistive load multiplied by a factor of 10 for display purposes. Finally, the third graph shows the active power of $500W$ that is supplied to the load.

The first and second graphs of Fig. 3.25 show the modulation waveforms for both the Half-Bridge inverter and active decoupling stages respectively (m_{inv} and m_b). Fig. 3.26

Table 3.4. Simulation parameters for the open-loop simulation of the DC/AC converter with dependent active power decoupling as a forming converter.

Parameter	**Symbol**	**Value**	**Unit**
Half-Bridge output voltage	V_o	127	V_{rms}
PV system voltage	V_{in}	205	V_{avg}
DC-link voltage	V_{dc}	450	V_{avg}
Voltage ripple on the DC-link	ΔV_{dc}	100	V
Rated power	P_o	500	W
Half-Bridge LC inductor	L_{inv}	1	mH
Half-Bridge LC capacitor	C_{inv}	7.3	μF
Load resistance	R_L	50	Ω
DC-link capacitor	C_{dc}	30	μF
PV systems' capacitor	C_{in}	2.2	μF
Transfer inductor	L_b	1	mH
Switching frequency of Half-Bridge stage	$f_{s_{HB}}$	50	kHz
Switching frequency of Boost stage	f_{s_B}	50	kHz

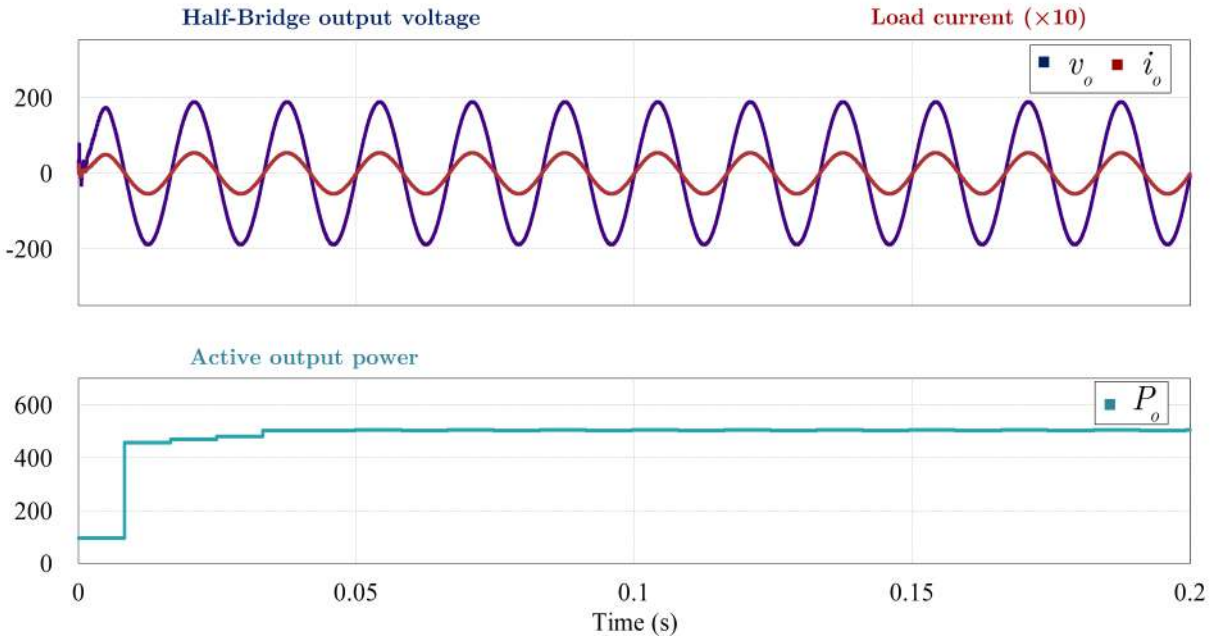


Figure 3.24. Half-Bridge output voltage and current and active power supplied to the load.

shows the frequency spectrum for both waveforms. It can be clearly remarked these waveforms are not purely sinusoidal and constant respectively as expected in a standard Half-Bridge inverter and a typical Buck-Boost converter.

It can be seen in Fig. 3.26 that m_{inv} holds the 2nd and 3rd harmonics besides the fundamental component at ω_0. This characteristic is employed to mitigate the ripple voltage effects due to the 2nd harmonic presented on the DC-link that could be present on the Half-Bridge inverter's output and then guarantee a low THD_v. As it is shown in the

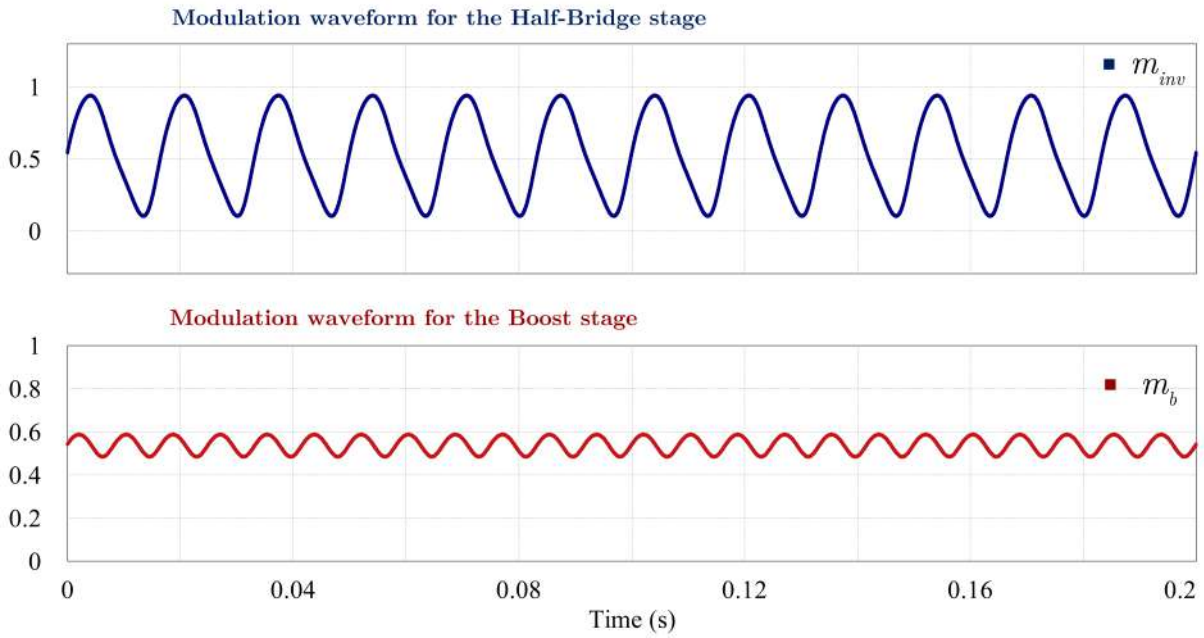


Figure 3.25. Modulation waveforms for both Half-Bridge and active decoupling stages.

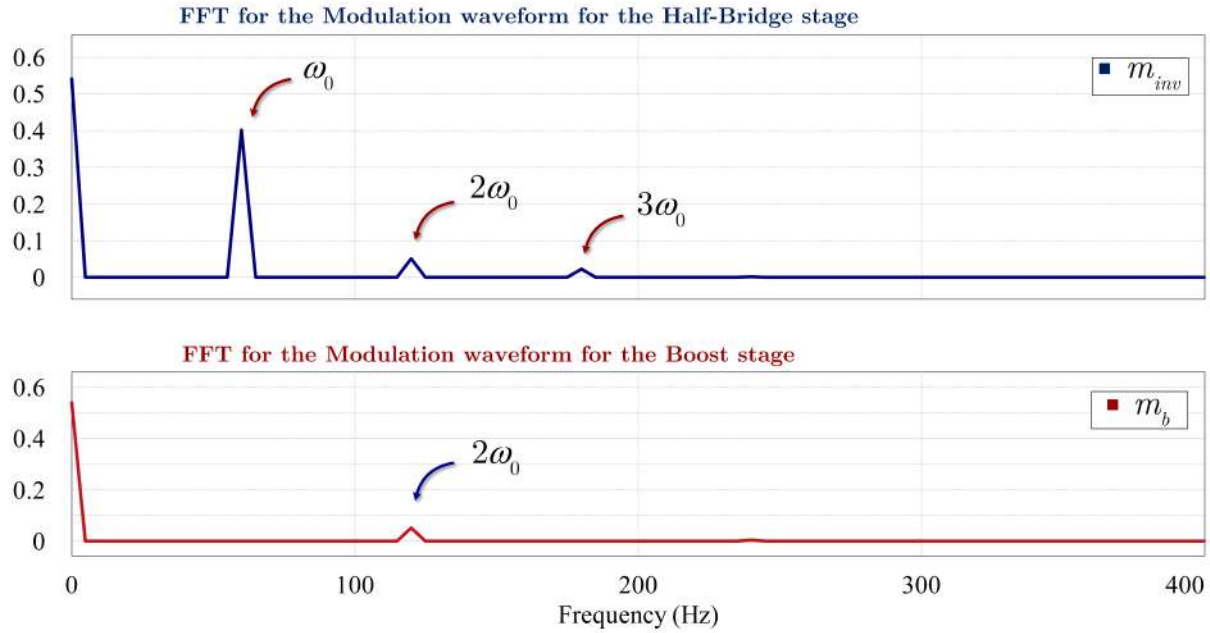


Figure 3.26. Frequency spectrum for the modulation waveforms for both Half-Bridge and active decoupling stages.

second graph of Fig. 3.25, the modulation waveform for the active decoupling stage m_b is not constant as expected in most DC/DC power converters, this is because this waveform holds the 2nd harmonic at $2\omega_0$ in order to buffer the effect of the ripple voltage on the PV system voltage by diverting it to the DC-link capacitor. After obtaining the modulation

waveforms, a $SPWM$ is employed for the power switches.

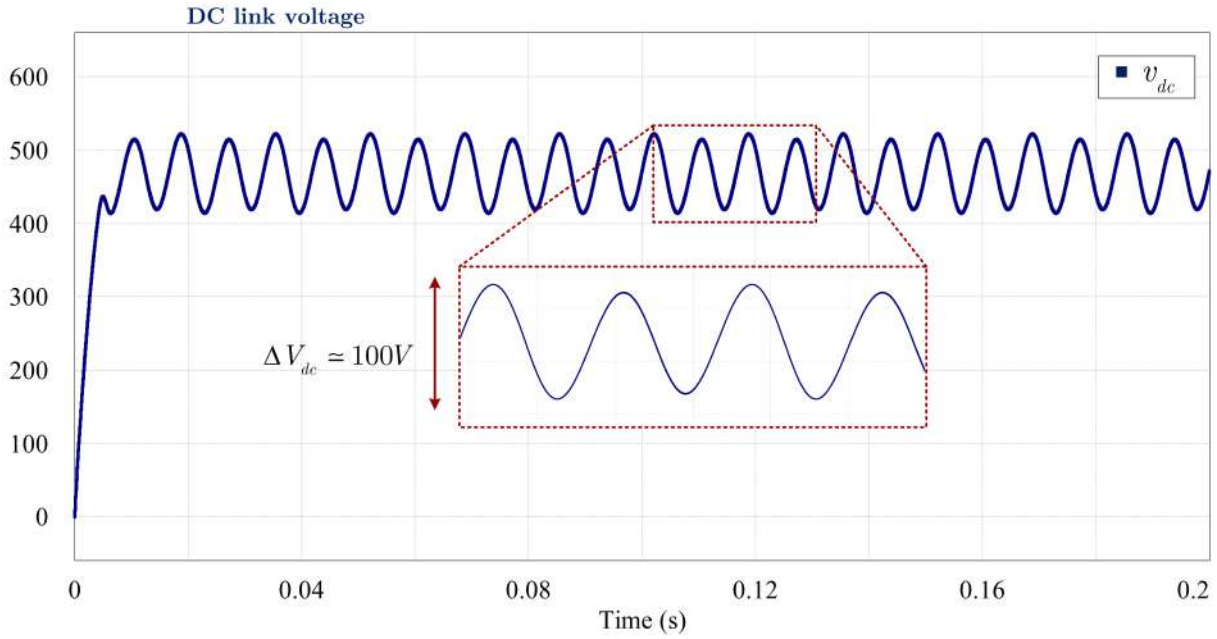


Figure 3.27. DC-link voltage.

Fig. 3.27 shows the DC-link voltage that reaches an approximate average value of $450V$ with a voltage ripple of $100V_{pp}$. A slight deviation in the average value can be distinguished due to the absence of the controller. On the other hand, Fig. 3.28 shows the voltage in the photovoltaic system that reaches the equilibrium point defined at an approximate value of $205V$ in steady-state. It can be distinguished that the voltage ripple reaches an approximate value of $2.5V_{pp}$. As a result of these simulations, it can be concluded that the converter operates adequately since it guarantees a low ripple voltage at the terminals of the photovoltaic system and also fulfills the task of a forming inverter reproducing a sinusoidal waveform at the output with the established parameters.

Fig. 3.29 shows the current across the inductor of the LC filter of the Half-Bridge inverter and the current through the decoupling Boost inductor. It can be seen that the current i_{inv} does not have a purely sinusoidal behavior and this is because there is no control loop in this simulation. It should be remarked that the current ripple can be minimized by increasing the switching frequency or by increasing the value of the inductor L_{inv}.

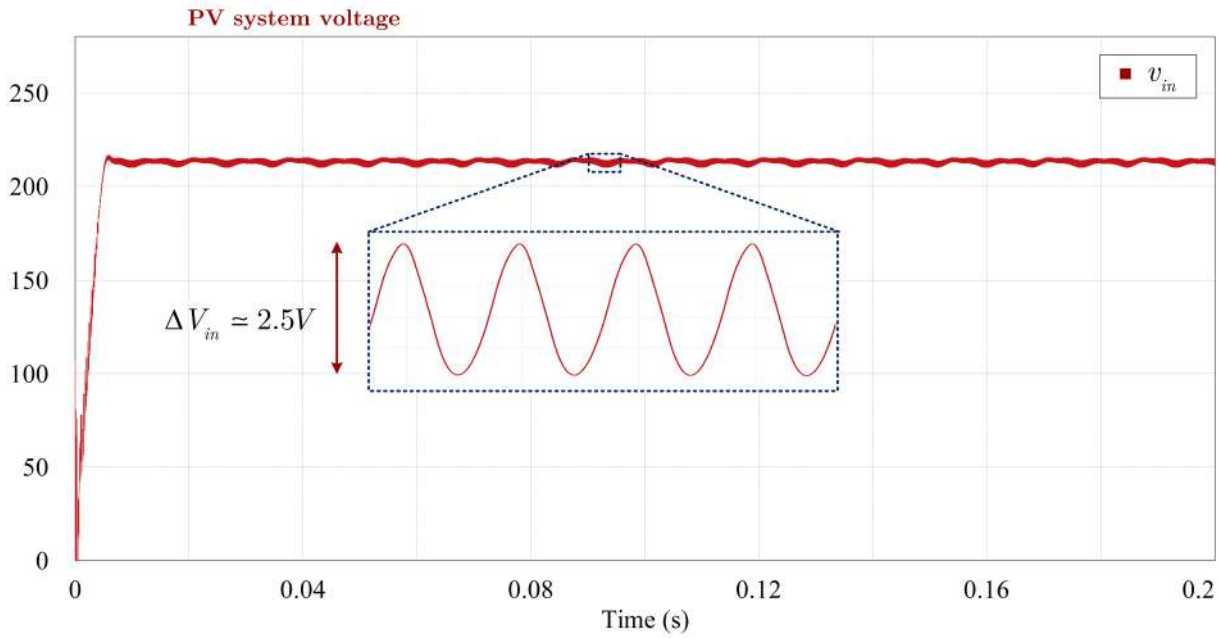


Figure 3.28. Photovoltaic system voltage.

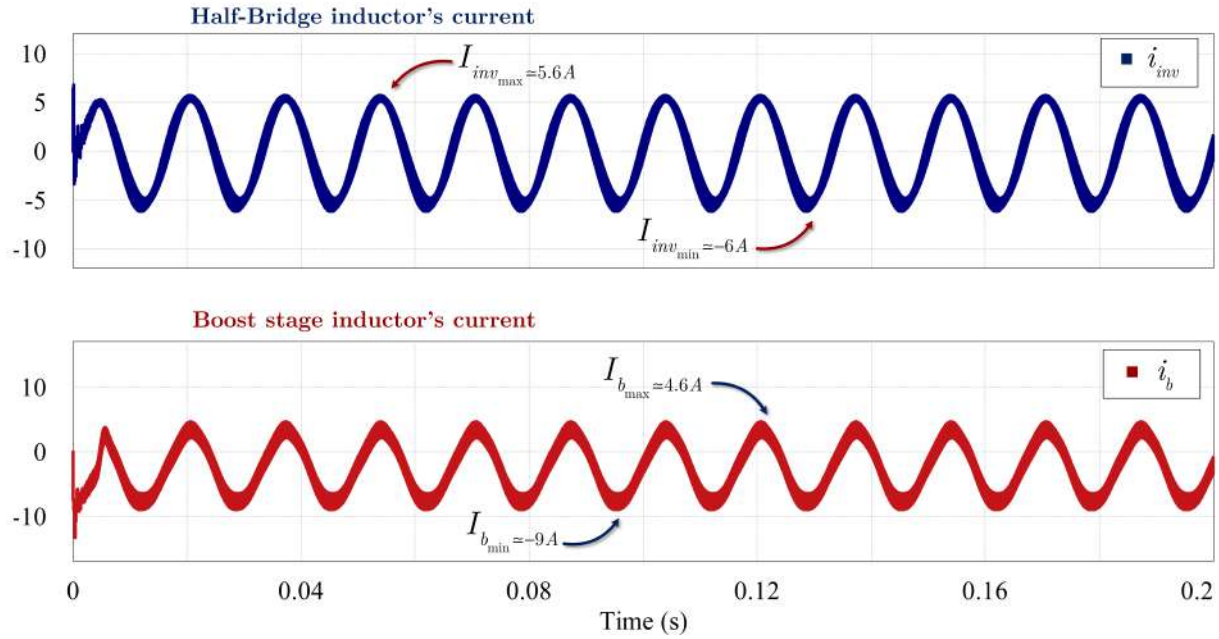
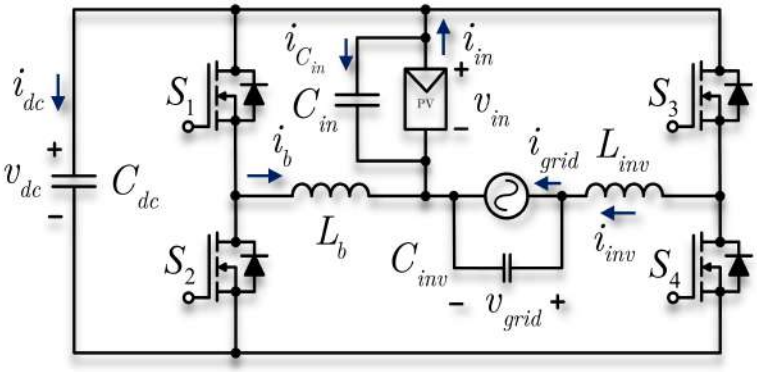


Figure 3.29. Half-Bridge inductor's current (i_{inv}) and Boost stage inductor's current (i_b).

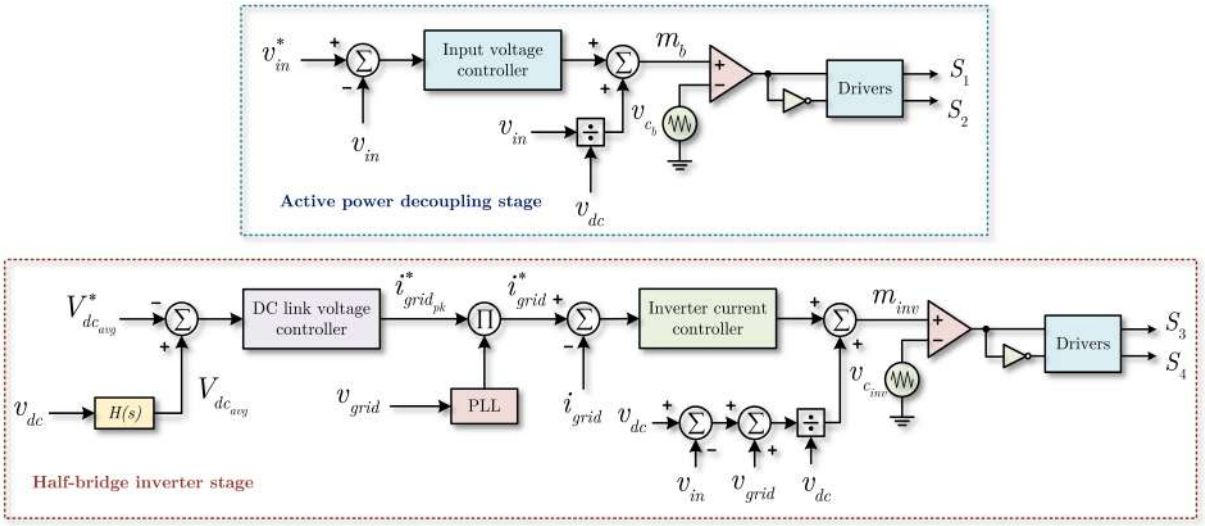
3.2.2. Closed-loop simulation for the DC/AC converter with dependent active power decoupling as a feeding converter

This simulation scenario aims to validate the operation of the converter operating in closed-loop as a feeding converter interconnected to the grid. The evaluated scheme is

shown in Fig. 3.30-(a) while Fig. 3.30-(b) shows the control system and the modulation scheme for the addressed simulation. The simulation sequence is shown in Fig. 3.31.



(a) DC/AC converter with dependent active power decoupling.



(b) Control and modulation schemes for the raised simulation.

Figure 3.30. Closed-loop simulation scenario for the DC/AC converter with active power decoupling.

1. From 0 to $t_1 = 0.4s$, the converter operates at the rated power ($500W$). The irradiance is fixed at a value of $1000W/m^2$.

2. At time $t_1 = 0.4s$, the irradiance is halved. This causes the panel to only be able to produce $200W$.

3. Finally, at time $t_2 = 0.8s$, an irradiance increase of 25% is performed to supply $400W$.

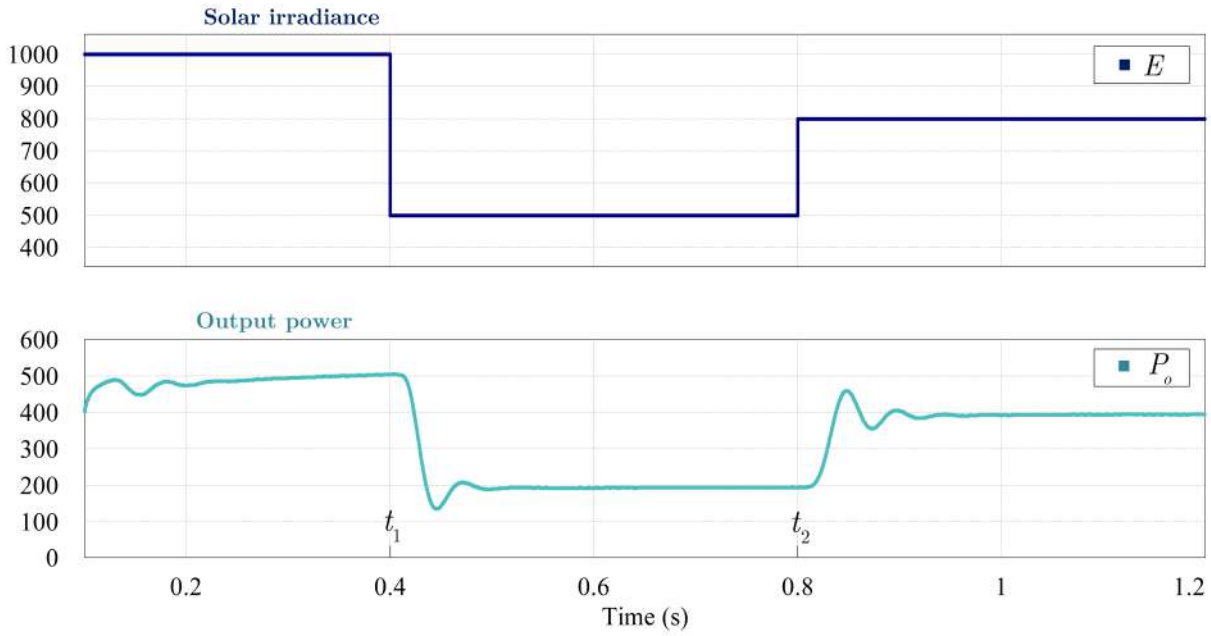


Figure 3.31. Irradiance and active power change sequence.

In Fig. 3.32 the grid voltage is shown against the reference obtained from the PLL. In this graph, it can be seen how the PLL is synchronized to the grid in approximately two cycles that correspond to a time of $33ms$.

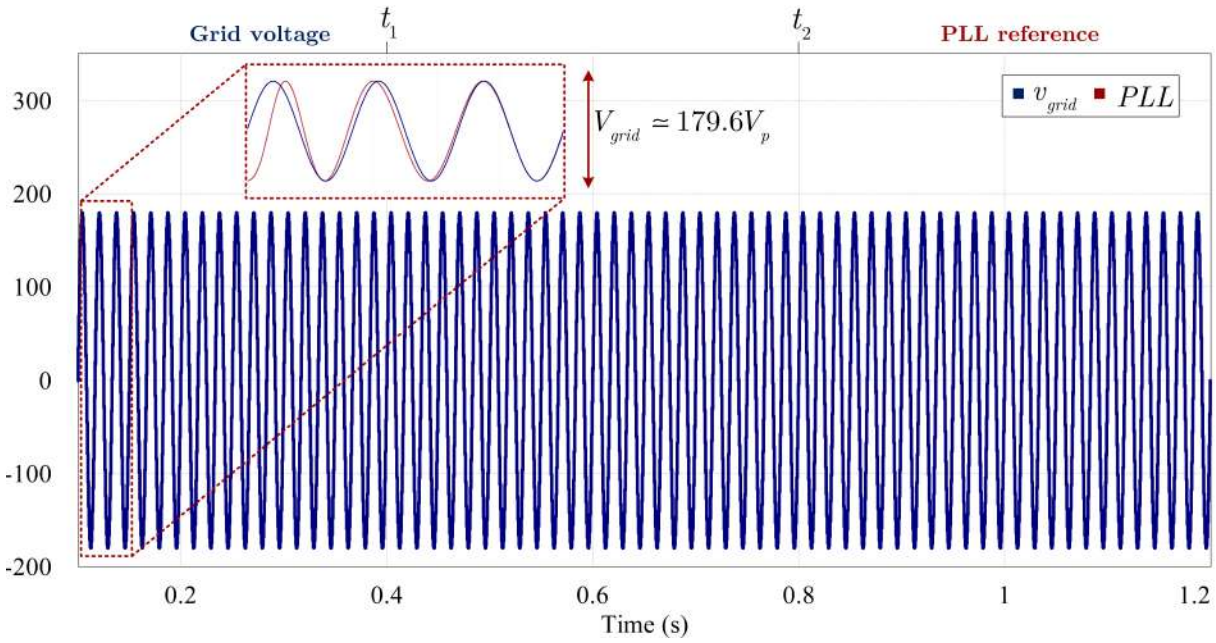


Figure 3.32. Grid voltage and PLL sync reference.

In Fig. 3.33 the instantaneous voltage on the DC-link is shown. One of the control objectives consists of guaranteeing a regulated average voltage level at the DC-link

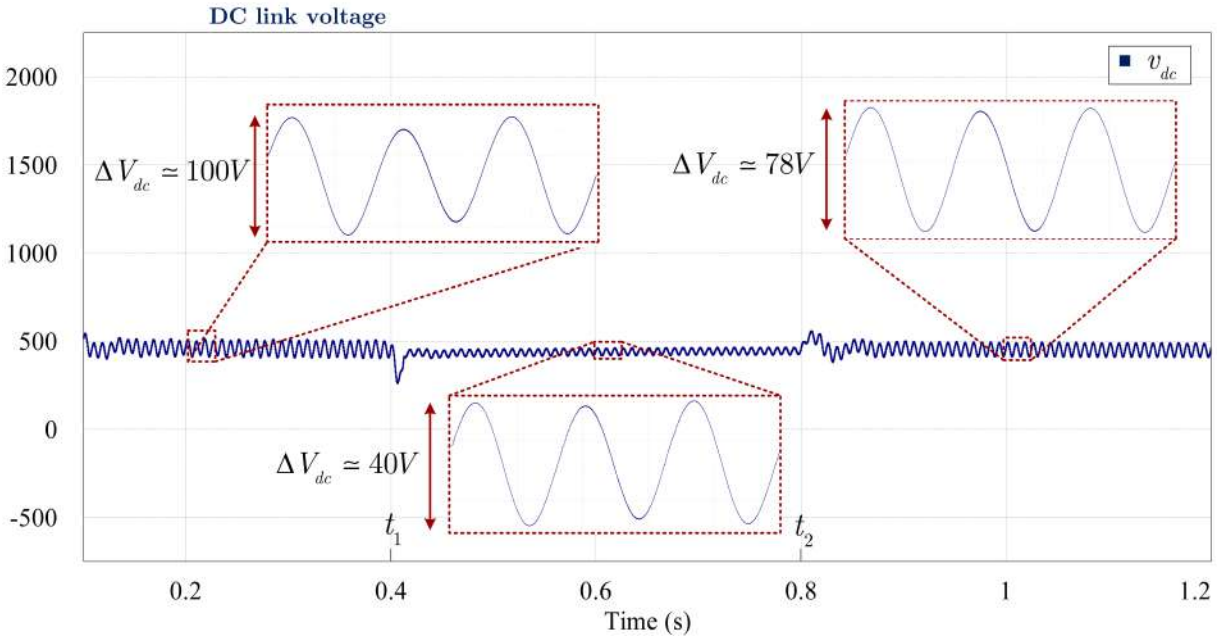


Figure 3.33. DC-link voltage in closed-loop.

terminals but allowing the ripple voltage to vary with the justification that a constant and reduced ripple voltage at the photovoltaic system terminals can be guaranteed. However, the maximum allowable oscillation on the DC-link is bounded as it is limited by the maximum allowable voltage in the semiconductor devices. As expected, from 0 to t_1, the ripple voltage is approximately $100V_{pp}$ operating at nominal power. At the instant of time t_1, the ripple voltage is reduced, but the average value is maintained (view Fig. 3.34). This happens because the supplied power to the electrical grid is lower and therefore the ripple voltage in the photovoltaic system is also lower. This causes the capacitor C_{dc} to store less energy and therefore the ripple level decreases; this is where it can be seen that there is a proportional relationship between the power level and the magnitude of the ripple voltage. Finally, at the instant of time t_2, the ripple voltage on the DC-link increases to $78V_{pp}$ because a power of $400W$ is now supplied to the grid; however, it can be seen that the average value remains regulated at all times at a value close to $450V$.

Fig. 3.35 shows the voltage of the photovoltaic system. One of the control objectives consists of keeping the average value regulated in the photovoltaic system and guaranteeing a low ripple voltage. In this figure, it can be observed that despite the disturbances in the irradiance changes, the average voltage in the photovoltaic system remains regulated at a value close to $20V$, as expected. In addition, despite the disturbances, the ripple level does not increase in any of the cases, since the ripple energy is stored in the DC-link capacitor (C_{dc}), and, this way, the variation is compensated.

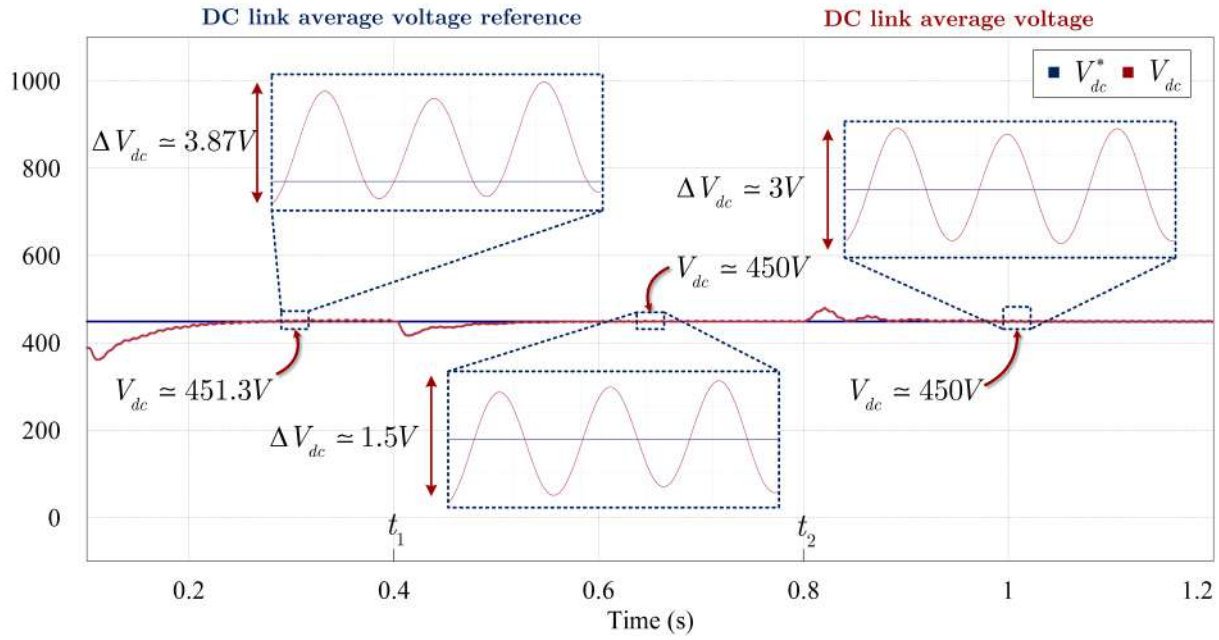


Figure 3.34. DC-link average reference and actual voltages.

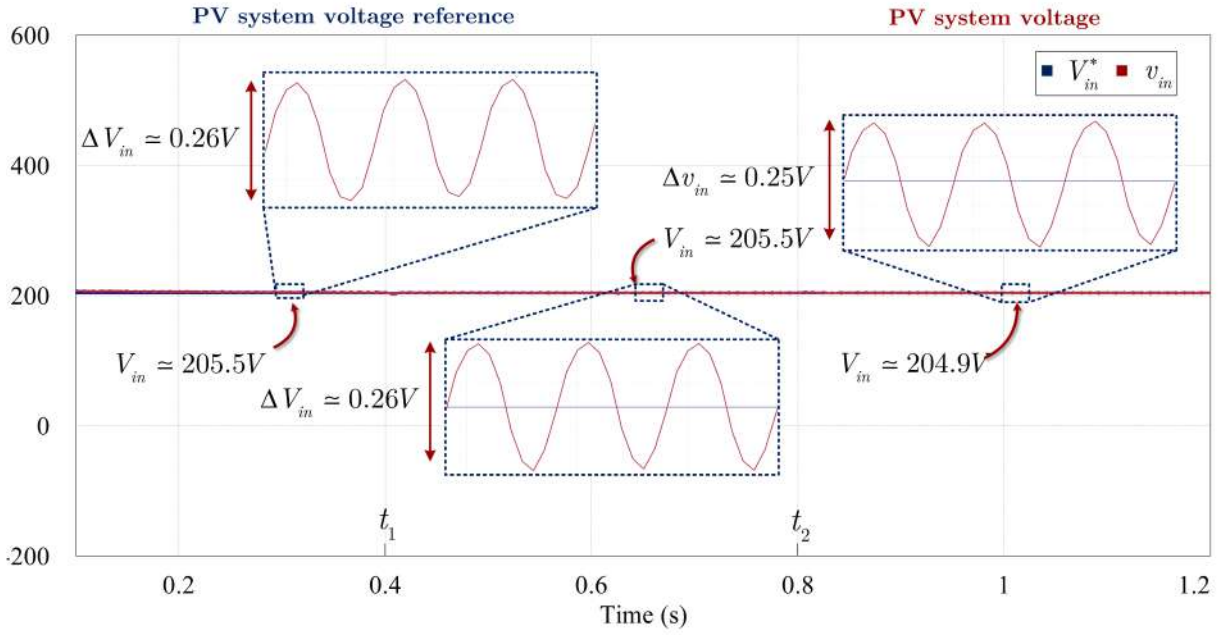


Figure 3.35. Photovoltaic system reference and actual voltages.

Finally, Fig. 3.36 shows the current supplied to the electrical grid compared to its reference. It can be seen that in all the periods, the control system adequately reproduces the reference current, obtaining a maximum current error of $0.13A$, corresponding to an approximate error of 0.66%. In addition, the longest response time obtained was around $t_r = 13ms$, which corresponds to the time-lapse when the first disturbance is occasioned

(t_a) and the time when the controller manages to stabilize the actual current (t_b)(view Fig. 3.36). Regarding the harmonic distortion in the current, a maximum distortion level of 4.19% was recorded.

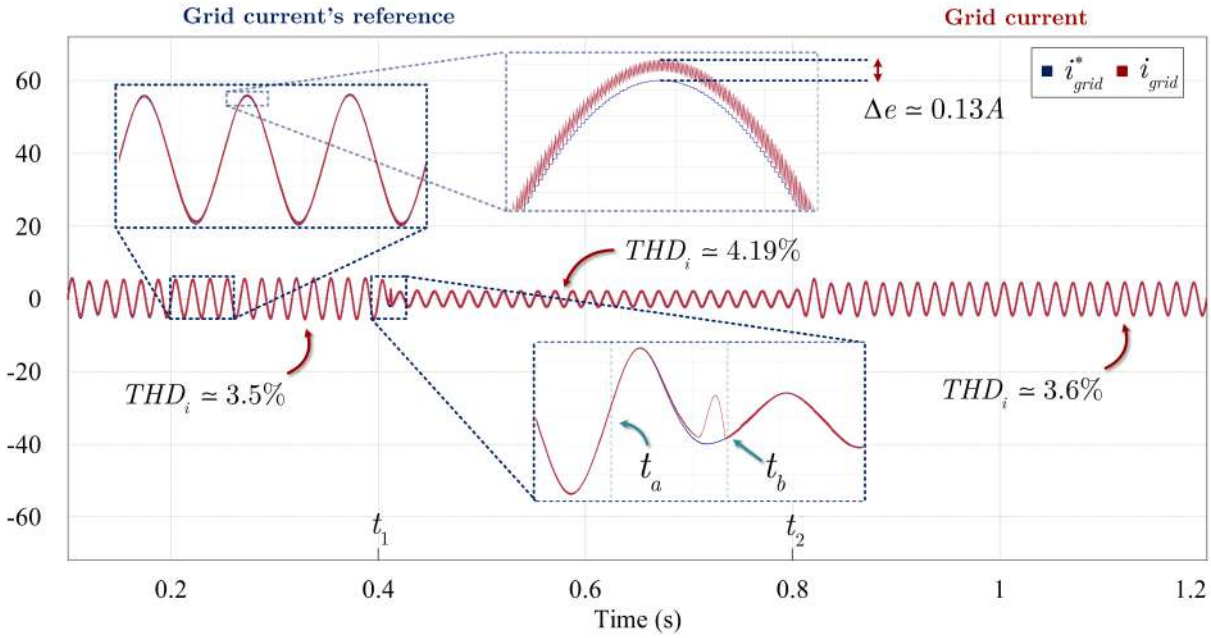
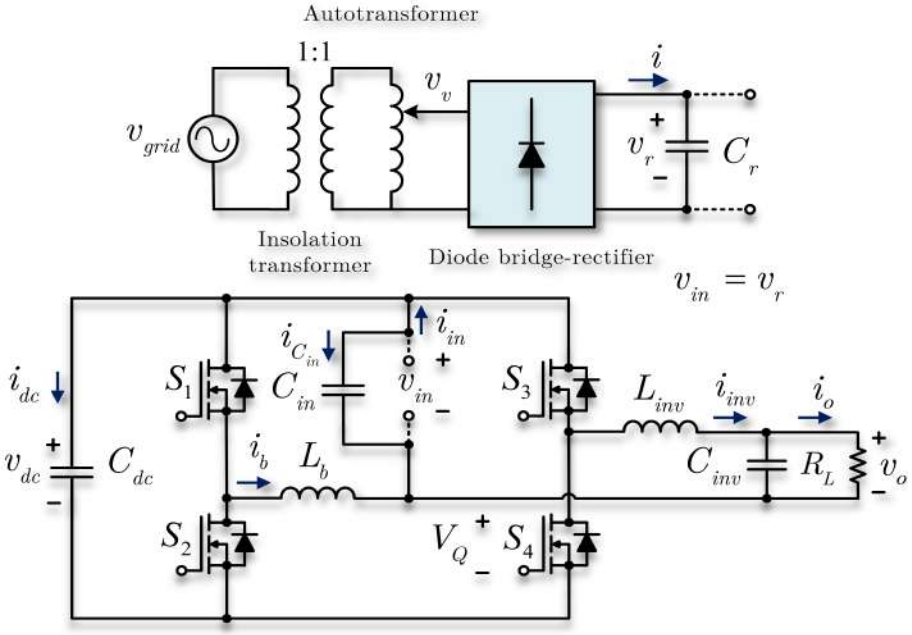


Figure 3.36. Grid reference and actual currents.

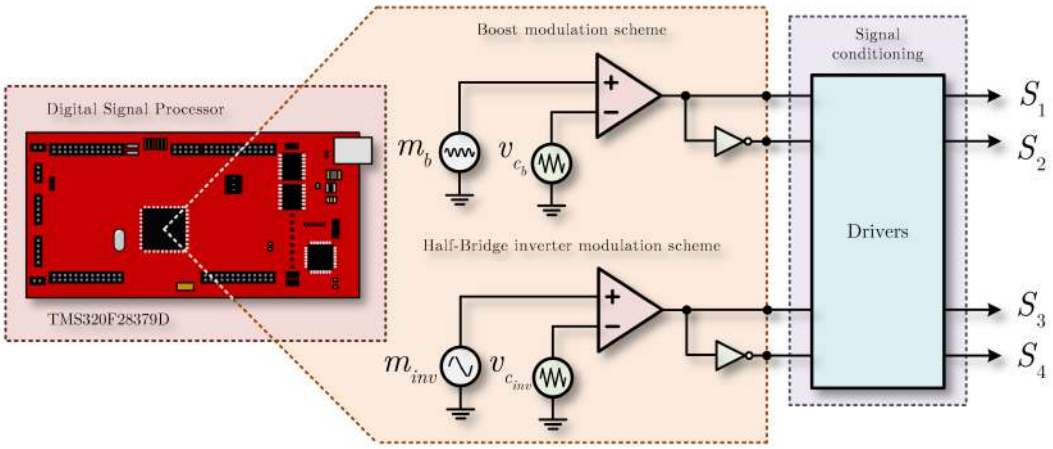
3.2.3. Open-loop experimental scenario for the DC/AC converter with active power decoupling

This experimental scenario aims to validate the operating principle of the converter in an open-loop scenario for the rated power conditions. The proposed scenario is shown in Fig. 3.37-(a) while Fig. 3.37-(b) shows the modulation schemes for the proposed experimental scenario; it can be highlighted that the switching signals come from different modulation schemes since the m_b and m_{inv} meet different tasks.

This scheme consists of the DC/AC converter with the dependent active power decoupling function in which a purely resistive load is connected to supply active power. For practicality reasons, a diode full-wave rectifier is connected as the input source to provide the input voltage source. In order to regulate the input voltage, an autotransformer is used and an isolation transformer is used to galvanically decouple the electrical grid from the power circuit. The parameters for this experimental scenario are shown in Table 3.5. These parameters were raised for the same simulation conditions of the power converter and this approach was addressed in depth in Chapter II, section 1.4.



(a) Experimental scenarios of a DC/AC converter with active power decoupling.



(b) Modulation scheme for the proposed experimental scenario.

Figure 3.37. Experimental scenario for the DC/AC converter with dependent active power decoupling.

Table 3.5. Experimental parameters for the DC/AC converter with dependent active power decoupling.

Parameter	**Symbol**	**Value**	**Unit**
Output voltage	V_o	127	V_{rms}
Input voltage	V_{in}	205	V_{avg}
DC-link voltage	V_{dc}	450	V_{avg}
Voltage ripple on the DC-link	ΔV_{dc}	100	V_{pp}
Rated power	P_o	500	W
Inverter filter's inductor	L_{inv}	1	mH
Inverter filter's capacitor	C_{inv}	7.3	μF
Load resistance	R_o	32	Ω
Link capacitor	C_{dc}	30	μF
Input capacitor	C_{in}	3.3	μF
Diode bridge rectifier's capacitor	C_r	1,100	μF
Boost inductor	L_b	1	mH
Switching frequency of the Half-Bridge inverter stage	$f_{s_{HB}}$	50	kHz
Switching frequency of Boost converter stage	f_{s_B}	50	kHz

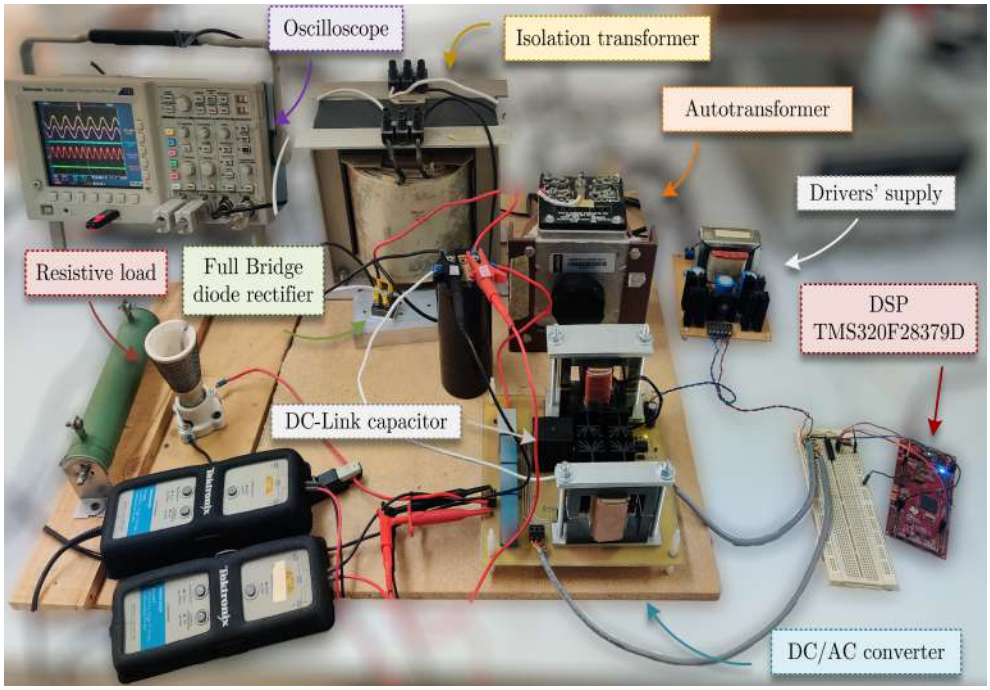
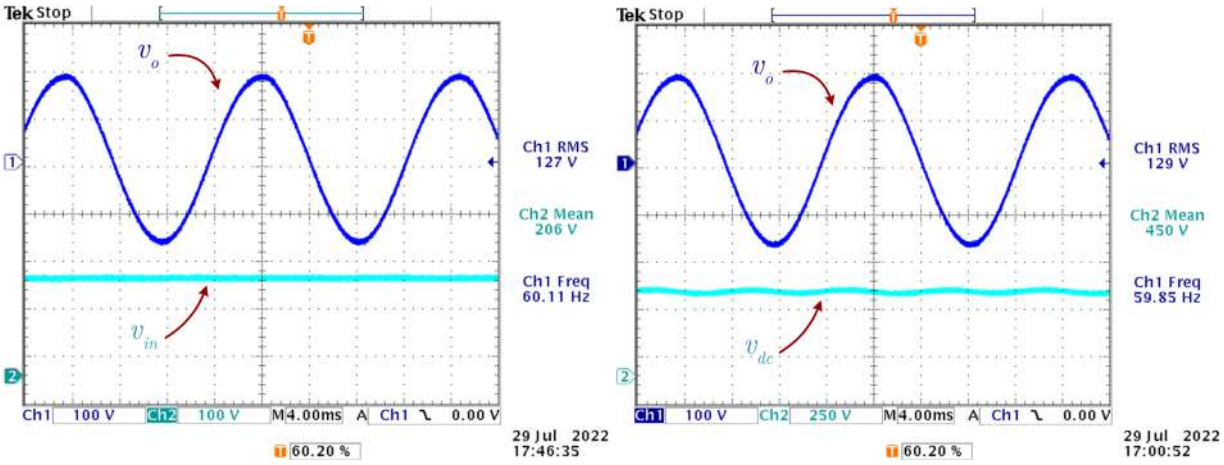


Figure 3.38. Experimental test bench.

Fig. 3.38 shows the built experimental test bench for the scheme raised in Fig. 3.37.

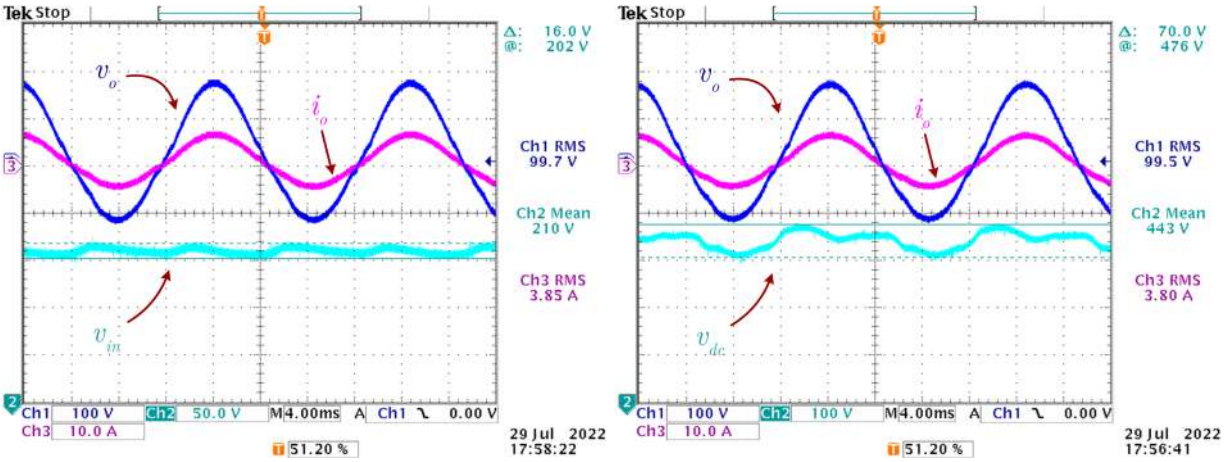
In Fig. 3.39 the converter operates without load. In channel 1, the voltage at the output of the inverter after the LC filter is displayed. The converter operates at the rated voltage level of $127V_{rms}$. Channel 2 shows the voltage at the converter's input. It can be noted that the ripple level is zero because there is no load connected. In Fig. 3.40 the voltage on the DC-link is shown in channel 2. This remains at an average value of $450V$ as expected.



(a) Output and input voltages.

(b) Output and DC-link voltages.

Figure 3.39. Converter operation with no load connected.



(a) Output and input voltages and output current.

(b) Output and DC-link voltages and output current.

Figure 3.40. Converter operation with the resistive load connected.

In Fig. 3.40 the resistive load of $R_o = 32$ is connected. It can be seen that immediately, a voltage ripple begins to appear in the input voltage v_{in}. Channel 2 of Fig. 3.40 shows how the converter performs the active decoupling task by transferring the ripple energy that shows up in the voltage v_{in} to v_{dc}, guaranteeing a low ripple voltage in what would correspond to the terminals of the photovoltaic system. It can be seen that the voltage at the inverter output decreased considerably when connecting the resistive load. This is an undesired phenomenon that is currently being studied to be resolved. Through the experimental results, the operating principle of the converter is validated since it managed to perform the task of active power decoupling and that of the half-bridge inverter.

From these experimental results, it can be concluded that DC/AC converter with active

power decoupling feature operates properly regarding the operation principle expected from the analysis and the simulations carried out since it has been capable to perform the Half-Bridge and the active power decoupling tasks at the same time.

Based on the experimental results obtained with the Bidirectional Buck-Boost converter, it was observed that the energy in the decoupling capacitor C_z was around $1.9J$, giving a normalized value of $E_{C_z} = 9.5mJ/W$, while in the work on which this converter was based it reaches $E_{C_z} = 13mJ/W$ [40]. The deviation is due to the fact that in [40], the capacitor C_z, the voltage level and the rated power are slightly larger; that is, $C_z = 150\mu F$ and $V_{z_{max}} = 295V$, $P_o = 500W$ respectively.

For the case of the DC/AC converter with dependent active power decoupling, the normalized energy in the DC-link capacitor resulted approximately in $E_{C_{dc}} = 7.5mJ/W$, while in [24], it reached $E_{C_{dc}} = 9mJ/W$. This deviation is also due to a discrepancy between the voltage and power levels worked between both experimental scenarios.

Regarding the efficiency of the Bidirectional Buck-Boost converter, some tests were carried out measuring the input and output voltages and currents at rated power to determine the efficiency, obtaining in the worst case an efficiency of 91%, which corresponds approximately to the values determined in the appendix B. It should be noted that these tests were performed before placing the snubber circuit. For the DC/AC converter, an approximate global efficiency of 88% was obtained, which fits the loss analysis addressed in section B.

As mentioned in Chapter II, the DC/AC converter with dependent active power decoupling can also operate as a conventional DC/AC full-bridge-based converter with typical passive decoupling. Fig. 3.41 shows in Channel 1 the inverter's PWM output voltage and the Math channel shows its harmonic content where it can be distinguished the characteristic harmonics for the typical unipolar SPWM. Channel 2 shows the LC filter output where it can be seen that a purely sinusoidal waveform with $THD_v \approx 1.52\%$ is obtained.

Finally, some measurements for estimating global efficiency were performed. Fig. 3.42-(a) shows in Channel 1 and 3 the voltage and current at the LC filter's output. Channel 2, displays the DC-link voltage while Channel 4 shows the input current, which corresponds to the rectifier input current. Finally, the Math channel computes the input active power supplied to the circuit which ranges around $638W$. In Fig. 3.42-(b), the same waveforms are shown, however, the output active power is displayed in the Math channel ($580W$).

Considering the input and the output active power, the global efficiency can be

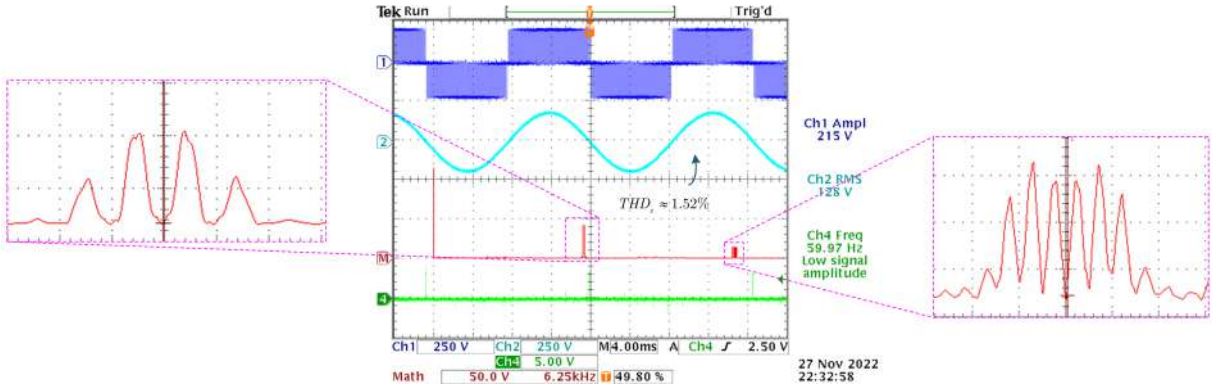
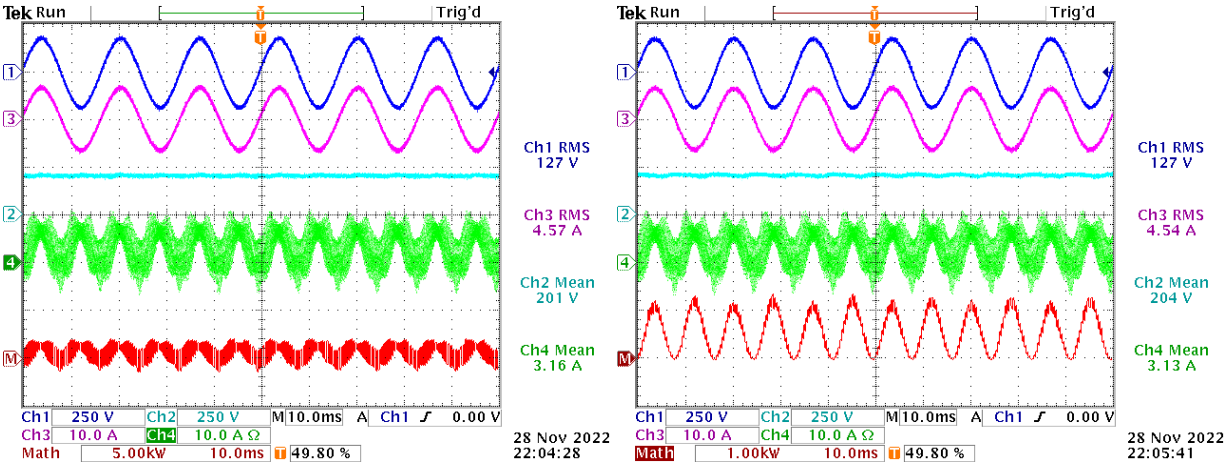


Figure 3.41. Typical DC/AC unipolar inverter waveforms.



(a) (b)

Figure 3.42. DC/AC converter operating at a power of $P_o = 580W$.

estimated by these measurements as follows:

$$\eta = \frac{P_{out}}{P_{in}} \times 100 = \frac{580}{638} \times 100 = 90.9\%. \tag{3.2}$$

Conclusions

In this thesis work, the study and synthesis of converters for active decoupling of power in low-voltage applications was addressed. This work aimed to provide a clear perspective of the operating principle of these types of schemes as an alternative to replace conventional passive decoupling schemes based on electrolytic capacitors and thus incorporate the use of film capacitors.

With the development of this work, the following conclusions can be established:

- Active power decoupling converters are useful schemes that are increasingly competing with passive power decoupling schemes due to the large number of advantages they possess; however, there are still important challenges to be resolved concerning the efficiency and the reliability. It is important to highlight then, to discern in the selection between an active or passive decoupling scheme and the type of scheme to select, a table of merit must be made considering the performance parameters of interest. Some parameters to consider are efficiency, reliability, cost, system complexity, volume, weight, power density, level of integration, power ranges, and application.

- Active power decoupling schemes based on power electronics converters can substantially reduce the total required equivalent capacitance on the DC-link for either AC/DC or DC/AC conversion schemes, since the operation and operability of two different topologies of active power decoupling converters could be validated in both simulation and experimental scenarios for AC/DC a DC/AC conversion schemes. By reducing the necessary capacitance, it is possible to use film capacitors that offer superior features than electrolytic capacitors such as longer lifespan, higher power density, lower losses due to their low series resistance, smaller volume and weight, and higher reliability.

- Active power decoupling schemes offer greater versatility than conventional passive decoupling schemes, since having active elements and a control scheme makes it possible to monitor and control the states of interest with high accuracy; in addition,

there is a great diversity of active power decoupling schemes for different types of applications.

- In active power decoupling schemes, the total required capacitance on the DC-link can be reduced by boosting the voltage and the ripple oscillations on the decoupling capacitor. Given this premise, it can be valid to consider to keep boosting the voltage with the aim of reducing the decoupling capacitor as much as desired. Nevertheless, this implies that the voltage ranges can exceed a boundary where isolation becomes a paramount issue; furthermore, there are eventually technological limits for the semiconductor devices to operate under certain voltage levels. Hence, it is important to delimit the suitable handy voltage levels for the desired application.

- Active power decoupling schemes aim to reduce the volume and weight of the decoupling scheme by reducing the DC-link capacitance. However, sometimes the volume and weight do not seem to differ too much from the traditional electrolytic capacitors, because there are more passive and active elements in active decoupling schemes than passive ones to perform the decoupling task. This can be true in some applications, nevertheless, if these two parameters are paramount issues, then there are some adjustments that can be performed to improve them. The inductor size can be reduced by increasing the switching frequency of the converter. If the isolation and the voltage ranges of the semiconductor devices are not a big concern, then the decoupling capacitor voltage can be boosted as much as desired and possible in order to reduce the total required capacitance on the DC-link. The efficiency of the power switches increased by selecting state-of-art devices and by applying soft switching methods which involves smaller heat sinks. The size of the PCB can be reduced as well by incorporating SMD packaging. Finally, if a proper PCB design is carried out, then the size can be optimized.

- Based on the analysis and the experimental results obtained, the Bidirectional Buck-Boost converter as an active power decoupling scheme turns out to be a suitable option since it manages to reduce the DC-link capacitor in a proportion of approximately 11 times the initial value of the DC-link capacitor. Taking into account the required decoupling capacitor of the Buck-Boost converter, the total equivalent capacitance can be reduced from $1,100\mu F$ to $200\mu F$, which represents a decrease of approximately 81.81% of the initial value; with only a $200\mu F$ capacitance required, the electrolytic capacitor can be replaced with film capacitors. In general, the Bidirectional Buck-Boost converter, since it can be used as an independent active power decoupling scheme, it is recommended to be used in applications where the

modularity characteristic is desirable, where a simple control scheme is required, and in systems in which the tasks of the main converters are not shared with the active power decoupling converter.

- The performance of the Bidirectional Buck-Boost converter is good enough to compete or even excel against the passive power decoupling scheme. In terms of efficiency, by using state-of-the-art semiconductor devices and using soft switching strategies that maximize efficiency, it is possible to directly compete with passive decoupling schemes. Regarding cost, there are device options with a good cost-performance ratio that can be used to obtain a final product at a competitive cost compared to the current cost of electrolytic capacitors.

- Initially, the Bidirectional Buck-Boost converter could operate under a conversion scheme where reactive power is managed by the power inverter to provide support to the network, however, there is a limitation regarding the amount of reactive power that could be managed due to the size reduced capacitor on the DC-link. In the case of harmonic currents, it would be necessary to consider having a control system that regulates the DC-link voltage when harmonic currents are injected into the grid; furthermore, the active power decoupling scheme must be dimensioned to manage this class of grid support functions.

- The DC/AC converter with a dependent active power decoupling feature is an excellent choice for reducing the total capacitance on the DC-link. From the simulation and experimental scenarios carried out with this converter, it can be concluded that this class of schemes is recommended to be used in applications where a higher level of integration and reduction of elements is sought by taking advantage of the characteristic of being a dependent active power decoupling scheme, the same active elements can be used to perform two different tasks. These types of schemes cannot be used in applications where modular active decoupling schemes are required, since this converter performs the active power decoupling task and the inverter task altogether. Even though the converter can manage reactive power, the amount of this is limited by the value of the DC-link capacitor and by the voltage level on it. Therefore, this converter is useful in applications where grid support is not a primary objective, since the support functions would be limited by the converter configuration and operating principle.

- Regarding the control schemes in both converters, favorable performances were obtained and the operation could be guaranteed against some disturbances caused.

The Buck-Boost converter operates under a very simple independent control scheme, which makes it very attractive for applications where simplicity and practicality are characteristics of interest; however, this control strategy does not consider the converter model, so certain dynamics of the converter behavior could be omitted, which could reduce the reliability of the control system; in addition, it is necessary to carry out a stability analysis to guarantee the dynamic ranges where the converter can operate properly.

Contributions

Based on the work carried out, the following contributions can be defined:

- A deep and clear conceptualization of the principle of operation of active power decoupling schemes.
- An extensive classification and quantitative evaluation of the most reported active power decoupling schemes, considering performance parameters such as efficiency, power levels, voltage levels, switching frequency, energy in passive elements, and the number of passive and active elements, among others.
- Analysis of the Bidirectional Buck-Boost converter as an active power decoupling scheme. A converter dimensioning methodology for passive and active elements. A validation in the simulation of open-loop and closed-loop scenarios. The design and construction of an experimental prototype of the converter and its validation in two open-loop test scenarios for an AC/DC and a DC/AC scheme. Finally, a quantitative and qualitative comparison of this active power decoupling scheme against the conventional passive power decoupling scheme based on an electrolytic capacitor.
- For the DC/AC converter with active dependent active power decoupling, its operating principle was analyzed in detail in the same way. The converter sizing methodology was presented and its operation principle in open-loop and closed-loop in a simulation scenario was validated. Finally, the experimental prototype was designed and built and open-loop tests were carried out, validating its correct operation.

Publications

Throughout the development of this thesis work, two publications were generated, which are listed below:

1. Yepez-Lopez, I., Cárdenas, V., Cruz-Velázquez, U., Miranda, H. & Alcalá, J. Bidirectional Buck-Boost converter as an Active Power Decoupling schema for Single-Phase Power Inverters. Memorias del Congreso Nacional de Control Automático, 2022.

2. Cruz-Velázquez, U., Cárdenas, V., Yepez-Lopez, I., González, M. & Alvarez-Salas, R. Operation Strategy for Photovoltaic Inverters with Microgrid Support Commuting from Grid-Feeding to Grid-Forming. Memorias del Congreso Nacional de Control Automático, 2022.

Open issues

Based on the challenges encountered during the development of the thesis work, the following issues are considered to continue with the line of research:

- Optimize the design and construction of the converters prototypes to avoid undesirable phenomena in the PCB such as overshoots in the drain-source voltage due to parasitic inductances.

- Implement more appropriate control systems based on the model to adopt the converter dynamics that are not contemplated.

- Carry out a stability analysis of the converters that allows visualizing the operating limits of the system.

- Implement the control systems developed to operate the converters prototypes in closed-loop and carry out experimental tests in case of disturbances.

- Carry out a quantitative and qualitative comparison between the two active decoupling schemes against the passive decoupling schemes and highlight the performance parameters of each one.

- Carry out a reliability analysis between the two active power decoupling schemes against the passive decoupling scheme in the face of a proposed general scenario.

APPENDIX A

Magnetic design

In this appendix the magnetic design and implementation of the inductors of both converters evaluated in this work are addressed. In the first instance, the design of the transfer inductor for the Bidirectional Buck-Boost converter is addressed. Then, the design for both inductors of the DC/AC converter with dependent active power decoupling is approached. Finally, the results of the design and construction of the inductors of both converters are shown; it should be noted that the inductors were designed and built by the author with the support of the Electrical Power Quality and Motor Control Laboratory of the UASLP.

A.1. Magnetic design for the Bidirectional Buck-Boost converter

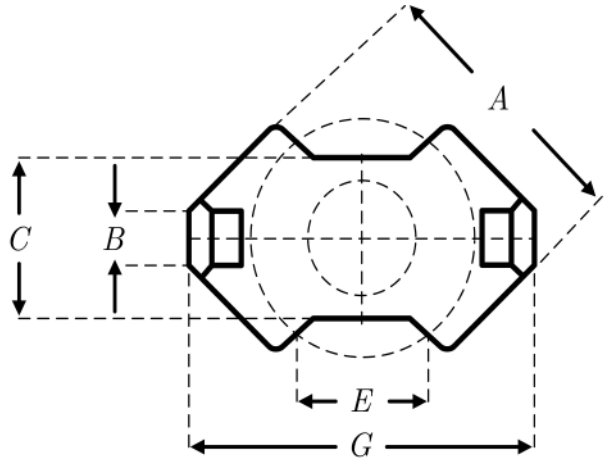
To carry out the magnetic design of the L inductor, it must be taken into account that the inductor operates in Discontinuous Conduction Mode (DCM); that is, the inductor's current is negative in a half-cycle. The electrical and magnetic parameters for the design are shown in Table A.1.

From Table A.1 it can be noted that the desired inductance is $620\mu H$ operating under a maximum current level of $5A_p$. These values come from the inductor sizing section in Chapter I, section 1.5.1. The selected core type is an RM14 type core of 3C95 ferrite material for a maximum flux density of $Bm = 0.45T$. the dimensions in mm for the core type RM14/I are shown in Fig. A.1 and Table A.2.

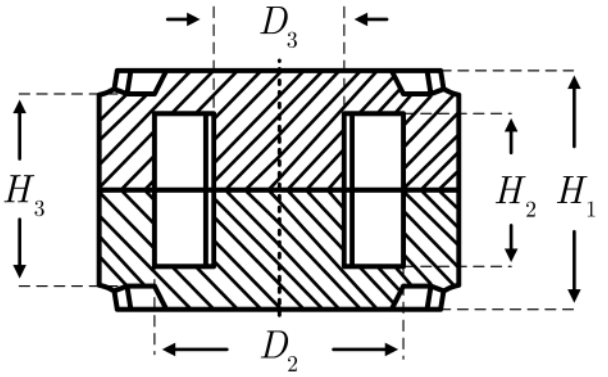
The magnetic design methodology is based on the work reported in [49]. The data from Tables A.1 and A.2 are employed for the design.

Table A.1. Parameters for the magnetic design of L.

Parameter	**Symbol**	**Value**	**Units**
Desired inductance	L	620	μH
Average current	$I_{L_{avg}}$	2.8	A_{avg}
Ripple current	ΔI_L	2.2	A_{pp}
Core type	–	RM14/I	–
Core material	–	3C95	–
Waveform coefficient	K_f	4.44	–
Window utilization factor	K_u	0.4	–
Temperature Constant	K_j	403	–
Cooling factor for temperature	y	-0.125	–
Geometry factor (ferrites) E-I	X	1.14	–
Magnetic flux density at 25°C and 100kHz	B_m	0.45	T
Window area	W_a	1.5184	cm^2
Effective cross-section of the core	A_c	1.6286	cm^2



(a) Top view.



(b) Front-side view.

Figure A.1. Physical dimensions for the RM14/I core.

Table A.2. Physical dimensions for the RM14/I core.

	A	B	C	D_2	D_3	E	G	H_1	H_2	H_3
Value	34.70	5.60	19.00	29.00	15.00	17.00	42.20	30.10	20.80	27.00

First, the maximum energy stored by the inductor can be determined as follows:

$$E_L = \frac{1}{2} L I^2 = 4.7mJ, \tag{A.1}$$

where $I = I_{L_{avg}} + \frac{\Delta I_L}{2}$.

The required area product considering the inductor's energy can be calculated in Eq. A.2.

$$A_p = \left(\frac{2E_L 10^4}{B_m K_u K_j} \right)^X = 1.3486cm^2. \tag{A.2}$$

From the dimensions in Table. A.2, it can be obtained the real area product (A_{p_r}) from the real physical dimensions of the core selected. It is important to remark that $A_{p_r} > A_p$ in order to be able to build the inductor; in case this premise is not fulfilled, then a bigger core should be selected.

$$A_{p_r} = W_a A_c = 2.4729cm^2. \tag{A.3}$$

The current density, J, stands for the amount of electric current flowing per unit cross-sectional area of a conductor. This can be computed as follows:

$$J = K_j A_p^y = 359.87A/cm^2. \tag{A.4}$$

Considering de current density and the *rms* current across the inductor L, it can be possible to compute the necessary American Wire Gauge (AWG) for the inductor wire as follows:

$$AWG = \frac{I_{rms}}{J} = 0.0108cm^2. \tag{A.5}$$

Considering the wire gauge selected, it is possible to obtain a first approximation of the initial number of winding turns. This parameter can be calculated in Eq. A.6.

$$N_I = \frac{W_a}{2AWG} = 70.05. \tag{A.6}$$

Considering the number of turns per cm^2 of the wire gauge selected ($AWG17 \rightarrow T_{cm^2} = 51.36$), it is possible to obtain the total number of winding turns as follows:

$$N_T = \frac{W_a T_{cm^2}}{2} = 38.99. \tag{A.7}$$

From this step, it can be proposed a specific number of winding turns for a particular air gap since this implies the final value of the ultimate flux density; it must be ensured

that the number of the proposed winding turns is less or at least equal to the number of the total winding turns, that is $N_p \leq N_T$. Then, a $N_p = 38$ is proposed. It must be then taken into account the maximum flux density that the core can withstand before saturating.

The air gap l_g and the real air gap $l_{g_{real}}$ can be computed as in Eqs. A.8 and A.9 respectively.

$$l_g = \frac{0.4\pi N_p^2 A_c 10^{-8}}{L} = 0.0477cm. \tag{A.8}$$

$$l_{g_{real}} = \frac{l_g}{2} = 0.0238cm. \tag{A.9}$$

Afterward, the number of the final winding turns is computed as follows:

$$N_f = \sqrt{\frac{Ll_g}{0.4\pi A_c m 10^{-8}}} = 34.9486, \tag{A.10}$$

where m stands for the fringing flux factor and can be expressed by Eq. A.11. G represents the winding length; that is $G = H_2$ (view Fig. A.1).

$$m = 1 + \frac{l_g}{\sqrt{A_c}} \ln\left(\frac{2G}{l_g}\right) = 1.2529. \tag{A.11}$$

Finally, from the air gap selected, the final maximum flux density must be verified by Eq. A.12 in order to avoid saturating the magnetic core.

$$B_{max} = \frac{LI}{N_f A_c 10^{-4}} = 0.4373T. \tag{A.12}$$

As can be observed in Eq. A.11, the maximum flux density obtained is fairly close to the rated flux density of the magnetic core selected; furthermore, it must be taken into account the real air gap that can be performed by the chosen material. In this case, two *Maylar* sheets of $14mil$ are performed as the new air gap ($l_g = 0.0711$). The Eqs. A.10, A.11 and A.12 can be then recalculated as in Eqs. A.13, A.14 and A.15.

$$m = 1 + \frac{l_g}{\sqrt{A_c}} \ln\left(\frac{2G}{l_g}\right) = 1.3551. \tag{A.13}$$

$$N_f = \sqrt{\frac{Ll_g}{0.4\pi A_c m 10^{-8}}} = 40, \tag{A.14}$$

$$B_{max} = \frac{LI}{N_f A_c 10^{-4}} = 0.3723T. \tag{A.15}$$

The final parameters for implementation are shown in Table A.3.

Table A.3. Parameters for the construction of L.

Parameter	**Symbol**	**Value**	**Units**
Real final inductance	L	625	μH
Wire gauge	AWG	17	–
Air gap	l_g	0.0711	cm
Final winding turns	N_f	40	–
Final maximum flux density	B_{max}	0.3723	T

It can be highlighted that the new maximum flux density is more suitable to work with since its value is much lower than the rated flux density of the magnetic core selected providing a safe operation margin and reducing the chances of saturating the core. It should remark that due to the presence of the skin effect due to the high switching frequency, it was decided to implement *Litz Wire* for the construction of the winding. Fig. A.2 shows the final result of the built inductor.

Figure A.2. Final results of the built inductor.

A.2. Magnetic design for the DC/AC converter with dependent active power decoupling

The DC/AC converter with dependent active decoupling requires two inductors for its operation. In Chapter 2, it was discussed that the inductor L_b is used to transfer the energy of the ripple voltage in terminals of the photovoltaic system toward the DC-link. On the other hand, the inductor L_{inv} together with the capacitor C_{inv} fulfill the function of the low-pass filter at the output of the Half-Bridge inverter. In this section, the magnetic design of the inductors L_b and L_{inv} is addressed. The parameters for the design are shown in Table A.4.

At first, it might be thought that the design methodology would be the same for both inductors since both seek to achieve an inductance of $1mH$ and the magnetic core is the same, however, the current level in L_b is greater than in L_{inv}. Then, at one point, the calculations can vary significantly. The physical dimensions are highlighted in Fig. A.3, where $D = 20.2mm$, $G = 27.9mm$, $E = 20.2mm$ and $F = 19.7mm$.

Table A.4. Parameters for the magnetic design of L_b and L_{inv}.

Parameter	**Symbol**	**Value**	**Units**
Desired inductance	L_b, L_{inv}	1	mH
Maximum current for L_b	I_{L_b}	15	A_p
Maximum current for L_{inv}	$I_{L_{inv}}$	6.5	A_p
Core type	–	E-80/38/20	–
Core material	–	Ferrite N-87	–
Waveform coefficient	K_f	4.44	–
Window utilization factor	K_u	0.4	–
Temperature Constant	K_j	590	–
Cooling factor for temperature	y	-0.125	–
Geometry factor (ferrites) E-N87	X	1.14	–
Magnetic flux density at 25°C and 100kHz	B_m	0.32	T
Window area	W_a	5.5103	cm^2
Effective cross-section of the core	A_c	3.9188	cm^2

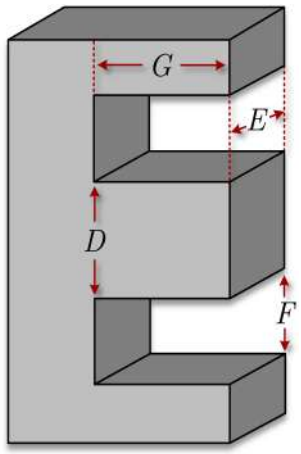


Figure A.3. Physical dimensions for a ferrite core N-87 E-80/38/20.

The design methodology used in section A.1 is the same used for L_b and L_{inv}. First, the maximum energy stored by the inductor L_b is determined as follows:

$$E_{L_b} = \frac{1}{2}LI^2 = 112mJ. \tag{A.16}$$

The required area product considering the inductor's energy and the real area product from the core dimensions are calculated respectively in Eqs. A.17 and A.18:

$$A_p = \left(\frac{2E_{L_b}10^4}{B_m K_u K_j}\right)^X = 47.91cm^2. \tag{A.17}$$

$$A_{p_r} = W_a A_c = 43.18cm^2. \tag{A.18}$$

It is clear from Eqs. A.17 and A.18 that the magnetic core does not have the area product required for the construction of the inductor. In order to address this issue, two joined cores are used to double the product of areas in order to comply with this constraint. In this way, Eq. A.18 can be recalculated as follows:

$$A_{p_r} = 2W_a A_c = 86.37cm^2. \tag{A.19}$$

Afterward, The current density, J is computed as follows:

$$J = K_j A_p^y = 337.91A/cm^2. \tag{A.20}$$

Even though the peak current is used to calculate the required area product, to determine the wire's gauge, the *rms* current across the inductor is taken into account, since this current is associated with heating due to winding losses. Considering then a current $I_{rms} = 6A$, the wire's gauge can be determined as follows:

$$AWG = \frac{I_{rms}}{J} = 0.0178cm^2. \tag{A.21}$$

Considering the wire gauge selected and the number of turns per cm^2 ($AWG14 \rightarrow T_{cm^2} = 26.14$), the initial and the total number of winding turns are determined in Eqs. A.22 and A.23 respectively; it is important to remark that the two cores are considered for these equations.

$$N_I = \frac{2W_a}{2AWG} = 310.33. \tag{A.22}$$

$$N_T = \frac{2W_a T_{cm^2}}{2} = 144.03. \tag{A.23}$$

Finally, by proposing an air gap of $l_g = 0.7cm$, the final number of turns N_f and the maximum flux density B_{max} can be determined in Eqs. A.24 and A.25 respectively. It can be observed that even though the maximum flux density equals the rated flux density of the magnetic core, it can still operate properly since the value is still permissible under the limits.

$$N_f = \sqrt{\frac{Ll_g}{0.4\pi A_c m 10^{-8}}} = 59. \tag{A.24}$$

$$B_{max} = \frac{LI}{N_f A_c 10^{-4}} = 0.3286T. \tag{A.25}$$

The same design methodology is applied for the inductor L_{inv}, however, from Eq. A.18 and knowing that the area product required for this inductor is $A_p = 7.1195$, it can be concluded that this inductor can be built with a single ferrite core. The parameters can be obtained through the same equations already analyzed. In this case, the breakdown of the calculations is omitted and the results are synthesized in Table A.5 along with the results for the inductor L_b.

Table A.5. Parameters for the construction of L_b and L_{inv}.

Parameter	**Symbol**	**Value**	**Units**
Real final inductance for L_b	L_b	1	mH
Real final inductance for L_{inv}	L_{inv}	1	mH
Wire gauge for L_b	AWG	14	–
Wire gauge for L_{inv}	AWG	17	–
Air gap for L_b	l_g	0.7	cm
Air gap for L_{inv}	l_g	0.35	cm
Final winding turns for L_b	N_f	59	–
Final winding turns for L_{inv}	N_f	62	–
Final maximum flux density L_b	B_{max}	0.3286	T
Final maximum flux density L_{inv}	B_{max}	0.2726	T

In Fig. A.4 the inductor L_{inv} built is shown. It can be seen that *Litz Wire* was also implemented for the construction of the winding to mitigate the skin effect.

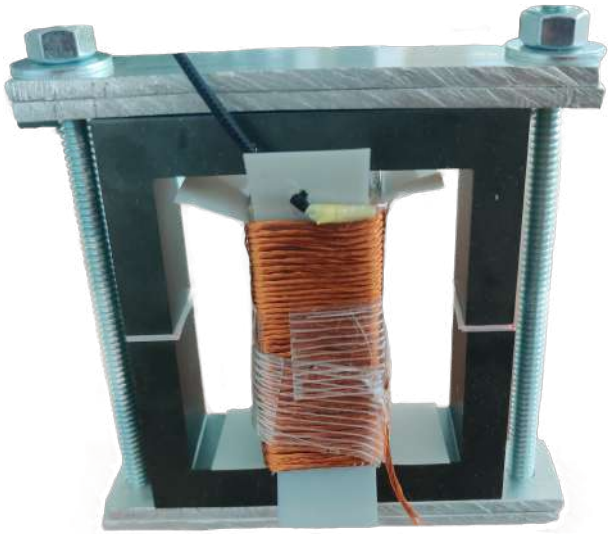


Figure A.4. Final results of the inductor L_{inv}.

APPENDIX B

Power losses analysis

In order to establish an adequate thermal design for the power switches and to be able to estimate the overall efficiency, a power losses analysis is addressed. This analysis aims to estimate the power losses in each power switch. First, the power losses analysis is carried out for the Bidirectional Buck-Boost converter and the DC/AC converter with dependent active power decoupling. Finally, a thermal design for a proper thermal sink selection is addressed.

B.1. Power losses on the Bidirectional Buck-Boost converter

Considering the voltage, current, and frequency parameters defined in chapter I for the operation scenario addressed, the power MOSFET IRFPS40N50L is selected since its performance parameters fit with the rated parameters for the converter operation. The parameters for the selected MOSFET are shown in Table B.1.

Table B.1. Parameters for the MOSFET IRFPS40N50L power losses analysis.

Parameter	**Symbol**	**Value**	**Units**
Drain-source voltage	V_{DS}	300	V
Drain-source current	I_D	5	V
Gate-source voltage	V_{GS}	12	V
Duty cycle	D	0.64	$-$
Switching frequency	f_{sw}	50	kHz
Drain-source on-state resistance	$R_{DS_{(on)}}$	0.1	Ω
Gate resistance	R_g	1	Ω
Turn-on delay time	$t_{d_{(on)}}$	27	ηs

Rise time	t_r	170	ηs
Turn-off delay time	$t_{d_{(off)}}$	50	ηs
Fall time	t_f	69	ηs
Total gate charge	Q_g	380	ηC
Gate-source charge	Q_{gs}	80	ηC
Gate-drain charge	Q_{gd}	190	ηC
Body diode rever recovery charge	Q_{rr}	1060	ηC
Input capacitance	C_{iss}	8110	pF
Output capacitance	C_{oss}	960	pF
Reverse transfer capacitance	C_{rss}	130	pF
Gate-drain capacitance	C_{gd}	130	pF
Gate-source capacitance	C_{gs}	7980	pF
Drain-source capacitance	C_{ds}	830	pF

The total power losses in a MOSFET can be defined in general by two terms considering that the MOSFET features the drain-source body diode; the first term ($P_{M_{total}}$) stands for the total power losses in the MOSFET without the influence of the body diode and is comprised of the switching, conduction, gate and output power losses; the second term consists of the total power losses ($P_{D_{total}}$) on the drain-source body diode which is comprised of the switching and conduction power losses. Tables B.2 and B.3 show the equations for the MOSFET and the body diode power losses.

In order to determine a high accuracy of the total losses in the MOSFET, the conduction, switching, gate, and output losses are considered and can be estimated by the equations shown in Table B.2. These equations are based on the methodology addressed in [50–54].

Table B.2. MOSFET power losses.

Power losses	**MOSFET losses equations**
Switching	$P_{M_{sw}} = \frac{1}{2} V_{DS} I_D \left(t_{ri} + t_{fv} + t_{fi} + t_{rv}\right) f_{sw}$
Conduction	$P_{M_{cond}} = I^2_{F_{rms}} R_{DS_{(on)}} = I_D R_{DS_{(on)}} D$
Gate	$P_{M_g} = Q_g V_{GS} f_{sw}$
Output	$P_{M_{out}} = \frac{1}{2} C_{ds} V^2_{DS} f_{sw}$

where $t_{ri} + t_{fv} + t_{fi} + t_{rv}$ are the rise and fall voltage and current times for the POWER MOSFET during a switching period and can be estimated by following the approach addressed below.

Several MOSFET switching characteristics are influenced by the actual value of the gate threshold and *Miller plateau* voltages. In order to calculate the Miller plateau voltage, one possibility would be to use the gate-to-source threshold voltage and transconductance of the MOSFET as listed in the datasheet. Unfortunately, the threshold is not very well defined. A more accurate method to obtain the actual ($V_{GS_{(th)}}$) and Miller plateau voltages ($V_{GS_{(sp)}}$) is to use the typical transfer characteristics curves of the datasheet.

In the first instance, the graph of the gate-source voltage (V_{GS}) against the drain current (I_D) is taken into account, and two different points of voltage V_{GS} are selected and the corresponding ones of the current I_D are extracted (view Fig. B.1). Therefore if $V_{GS_1} = 4.5V$ and $V_{GS_2} = 5.5V$, then $I_{D_1} = 7A$ and $I_{D_2} = 30A$.

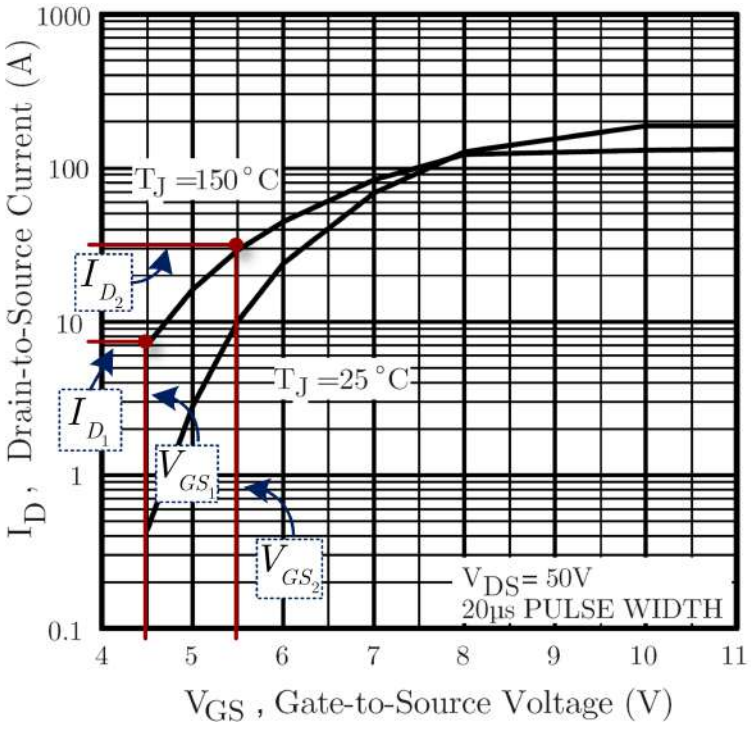


Figure B.1. Typical transfer characteristics.

From the voltage and current points obtained, the gate-source threshold voltage ($V_{GS_{(th)}}$) and the gate-source *miller plateau* voltage ($V_{GS_{(sp)}}$) can be calculated in Eqs. B.1, B.2 and B.3:

$$V_{GS_{(th)}} = \frac{V_{GS_1}\sqrt{I_{D_2}} - V_{GS_2}\sqrt{I_{D_1}}}{\sqrt{I_{D_2}} - \sqrt{I_{D_1}}} = 3.56V, \tag{B.1}$$

$$V_{GS_{(sp)}} = V_{GS_{(th)}} + \sqrt{\frac{I_D}{K}} = 4.35V, \tag{B.2}$$

where K can be calculated as follows:

$$K = \frac{I_{D_1}}{\left(V_{GS_1} - V_{GS_{(th)}}\right)^2} = 8.0172. \tag{B.3}$$

Subsequently, the rise and fall voltages and current times for the POWER MOSFET ($t_{ri} + t_{fv} + t_{fi} + t_{rv}$) can be computed in Eqs. B.4, B.5, B.6 and B.7 respectively.

$$t_{ri} = R_g C_{gs} \ln \frac{V_{GS} - V_{GS_{(th)}}}{V_{GS} - V_{GS_{(sp)}}} = 0.78\eta s. \tag{B.4}$$

$$t_{fv} = R_g \frac{Q_{gd}}{V_{GS} - V_{GS_{(sp)}}} = 24.85\eta s. \tag{B.5}$$

$$t_{fi} = R_g C_{gs} \ln \frac{V_{GS_{(sp)}}}{V_{GS_{(th)}}} = 1.59\eta s. \tag{B.6}$$

$$t_{rv} = \frac{R_g Q_{gd}}{V_{GS_{(sp)}}} = 43.62\eta s. \tag{B.7}$$

Afterward, the power losses can be then calculated by applying the results of the rise and fall voltage and current times on the equations shown in Table B.2.

$$P_{M_{sw}} = \frac{1}{2} V_{DS} I_D \left(t_{ri} + t_{fv} + t_{fi} + t_{rv}\right) f_{sw} = 2.65W. \tag{B.8}$$

$$P_{M_{cond}} = I^2_{F_{rms}} R_{DS_{(on)}} = I_D R_{DS_{(on)}} D = 0.32W. \tag{B.9}$$

$$P_{M_g} = Q_g V_{GS} f_{sw} = 0.22W. \tag{B.10}$$

$$P_{M_{out}} = \frac{1}{2} C_{ds} V^2_{DS} f_{sw} = 1.8675W. \tag{B.11}$$

Finally, the total power losses on the MOSFET is the sum of all the above; i.e:

$$P_{M_{total}} = P_{M_{sw}} + P_{M_{cond}} + P_{M_g} + P_{M_{out}} = 5.07W. \tag{B.12}$$

A similar procedure for estimating the drain-source body diode power losses is performed. Table B.3 shows the power losses for the body diode.

It should be highlighted from Table B.3 that it is necessary to calculate the dynamic diode resistance (R_{DT}) and the threshold diode voltage (V_{SD}) in order to obtain the conduction power losses. Furthermore, the average and the *rms* forward currents ($I_{F_{avg}}$

Table B.3. MOSFET's Body diode power losses.

Power losses	Drain-source body diode losses equations
Switching	$P_{D_{sw}} = \frac{1}{4} Q_{rr} V_{DS} f_{sw}$
Conduction	$P_{D_{cond}} = V_{TO} I_{F_{avg}} + I^2_{F_{rms}} R_{DT}$

and $I_{F_{rms}}$ respectively) are required. In this case, both were extracted from the simulation proposed for the power converter under rated power conditions.

Initially, the source-drain voltage (V_{SD}) against the reverse drain current is taken into account for estimating the threshold diode voltage (V_{TO}) and the diode dynamic resistance R_{DT}. In this case, if $I_{F_1} = 3A$ and $I_{F_2} = 40A$, then $V_{F_1} \approx 0.42V$ and $V_{F_2} = 0.95V$.

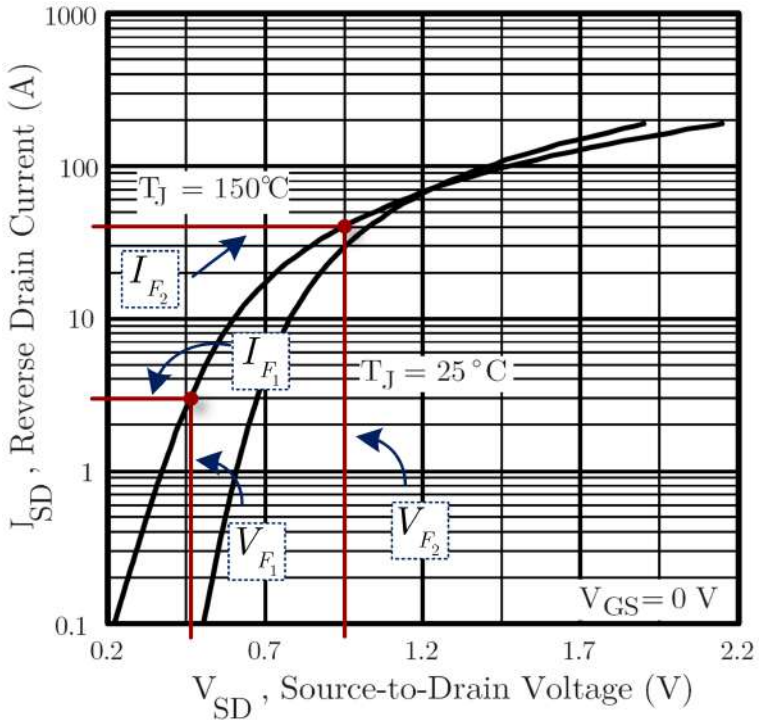


Figure B.2. Typical source-drain diode forward voltage.

Afterward, the dynamic resistance and the threshold voltage of the body diode can be calculated in Eqs. B.13 and B.14 respectively.

$$R_{DT} = \frac{V_{F_2} - V_{F_1}}{I_{F_2} - I_{F_1}} = 14.3m\Omega. \tag{B.13}$$

$$V_{TO} = \frac{V_{F_1} I_{F_2} - V_{F_2} I_{F_1}}{I_{F_2} - I_{F_1}} = 0.37V. \tag{B.14}$$

Finally, the diode power losses can be computed by applying the equations from Table B.3:

$$P_{D_{sw}} = \frac{1}{4} Q_{rr} V_{DS} f_{sw} = 3.97W, \tag{B.15}$$

$$P_{D_{cond}} = V_{TO} I_{F_{avg}} + I^2_{F_{rms}} R_{DT} = 0.39W. \tag{B.16}$$

The total power losses of the body diode are the sum of the two above, that is:

$$P_{D_{total}} = P_{D_{cond}} + P_{D_{sw}} = 4.37W. \tag{B.17}$$

The total device power losses considering the power losses of MOSFET and the drain-source body diode is then defined as:

$$P_{D_{total}} = P_{M_{total}} + P_{D_{total}} = 9.44W. \tag{B.18}$$

Considering that the power converter is sized to operate under a rated power of $P_{in} = 200W$ and only the power switches losses are considered and since the converter has only two power switches, the theoretical global efficiency can be calculated as follows:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{181.12}{200} \times 100 = 90.56\%. \tag{B.19}$$

B.1.1. Thermal design for the Buck-Boost converter

A proper thermal design is prominent to be able to select a proper heatsink for the power switches. Fig. B.3 shows the thermal equivalent circuit for the power transistor. T_J stands for the temperature at the semiconductor junction; T_C and T_S represents the case and the sink temperatures respectively, while T_A is the ambient temperature. Every union of the thermal circuit is represented by a thermal resistance which stands for the ability of the material to oppose the increase in temperature. $R_{\theta_{JC}}$ and $R_{\theta_{CS}}$ are typically given by the datasheet of the semiconductor device. P_d represents the total dissipated power by the semiconductor device; this parameter is obtained from the power losses analysis for the respective application.

The idea of the thermal design is to find a thermal resistance $R_{\theta_{SA}}$ such that the junction temperature complies with the maximum recommended to operate; i.e. $T_J \leq 125°C$. By finding $R_{\theta_{SA}}$, it is then possible to choose a proper heatsink for the semiconductor device and then, guarantee the junction temperature. the sink-ambient thermal resistance can be calculated as follows:

$$R_{\theta_{SA}} = \frac{T_J - T_A}{P_D} - R_{\theta_{JC}} - R_{\theta_{CS}}. \tag{B.20}$$

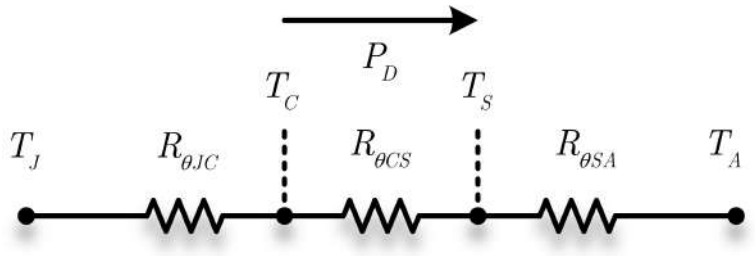


Figure B.3. Equivalent thermal resistive circuit.

Table. B.4 shows the parameters required for the thermal design, where P_D is obtained from the power losses analysis addressed in section B.1, while the thermal resistances are extracted from the datasheet of the MOSFET selected (IRFPS40N50L).

Table B.4. Parameters for the MOSFET IRFPS40N50 thermal design.

Parameter	**Symbol**	**Value**	**Units**
Dissipated power	P_D	9.44	W
Junction-case thermal resistance	$R_{\theta_{JC}}$	0.23	$°C/W$
Case-sink thermal resistance	$R_{\theta_{CS}}$	0.24	$°C/W$
Junction temperature	T_J	125	$°C$
Ambient temperature	T_J	40	$°C$

Considering the parameters from Table. B.4 and the Eq. B.20, the sink-ambient thermal resistance results as:

$$R_{\theta_{SA}} = \frac{T_J - T_A}{P_D} - R_{\theta_{JC}} - R_{\theta_{CS}} = 8.52°C/W. \tag{B.21}$$

Based on the thermal resistance obtained, a search and comparison of the different heatsink models were carried out in order to select the most suitable option for the raised thermal parameters. It was determined that PA-T2X-38E heatsink from the manufacturer Ohmite was the best choice for the application addressed.

B.2. Power losses on the DC/AC converter with active power decoupling feature

In order to establish an adequate thermal design for the switches of the DC/AC converter with active power decoupling feature, a power losses analysis is carried out to determine the total power dissipated in each of the devices. Considering the voltage, current and frequency parameters, it was decided to select the IGBT IXYP8N90C3D1. Table B.5 shows the parameters that were considered for the power losses analysis.

Table B.5. Parameters for the IGBT IXYP8N90C3D1 power losses analysis.

Parameter	**Symbol**	**Value**	**Units**
Maximum voltage on the DC-link	$V_{dc_{max}}$	550	V
Maximum current across the DC-link	$I_{dc_{max}}$	15	A
Turn-on delay time	$t_{d_{(on)}}$	20	ηs
Turn-off delay time	$t_{d_{(off)}}$	130	ηs
Switching frequency	f_s	50	kHz
Maximum saturation collector-emitter voltage	$V_{CE_{sat}}$	3	V
Body diode reverse recovery charge	Q_{rr}	400	ηC

The procedure to determine the power losses in the device is different from the procedure discussed in section B.1, since in this case, the switch used is an IGBT. However, the losses in the transistor and the losses in the antiparallel diode are taken into account in the same way [55, 56]. In the case of the transistor, the switching and conduction losses are considered. For the reverse diode, only switching losses are taken into consideration.

The switching losses can be determined at first by calculating the dissipated energy when the transistor is turning on (Eq. B.22) and off (Eq. B.23).

$$E_{on} = \left(\frac{t_{on}}{6}\right) I_{dc_{max}} \left(V_{dc_{max}} + 2V_{CE_{SAT}}\right). \tag{B.22}$$

$$E_{off} = \left(\frac{t_{off}}{6}\right) I_{dc_{max}} \left(V_{dc_{max}} + 2V_{CE_{SAT}}\right). \tag{B.23}$$

On the other hand, the energy when the transistor is conducting can be determined as follows:

$$E_{con} = V_{CE_{SAT}} I_{dc_{max}} t_{on}. \tag{B.24}$$

The dissipated power on the transistor can be obtained by multiplying the sum of the switching and conduction energies, that is:

$$P_{T_I} = E_{T_I} f_s, \tag{B.25}$$

where $E_{T_I} = E_{on} + E_{off} + E_{con}$.

The recovery diode power losses can be determined considering the reverse recovery charge, the DC-link voltage and the switching frequency as follows:

$$P_{D_I} = 0.25 Q_{rr} V_{dc_{max}} f_s. \tag{B.26}$$

Considering the parameters from Table B.5, it is possible to calculate the power losses of the IGBT by applying the Eqs. B.22-B.26.

$$E_{on} = \left(\frac{t_{on}}{6}\right) I_{dc_{max}} \left(V_{dc_{max}} + 2V_{CE_{SAT}}\right) = 27.8\mu J. \tag{B.27}$$

$$E_{off} = \left(\frac{t_{off}}{6}\right) I_{dc_{max}} \left(V_{dc_{max}} + 2V_{CE_{SAT}}\right) = 180\mu J. \tag{B.28}$$

$$E_{con} = V_{CE_{SAT}} I_{dc_{max}} t_{on} = 0.9\mu J. \tag{B.29}$$

$$E_{T_I} = E_{on} + E_{off} + E_{con} = 209.4\mu J. \tag{B.30}$$

$$P_{T_I} = E_{T_I} f_s = 10.47W. \tag{B.31}$$

$$P_{D_I} = 0.25 Q_{rr} V_{dc_{max}} f_s = 2.75W. \tag{B.32}$$

Finally, the total power losses for the device considering the recovery diode are:

$$P_{D_{total}} = P_{T_I} + P_{D_I} = 13.22W. \tag{B.33}$$

Considering that the power converter is sized to operate under a rated power of $P_{in} = 500W$ and only the power switches losses are considered and since the converter has only four power switches, the theoretical global efficiency can be calculated as follows:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{181.12}{200} \times 100 = 89.42\%. \tag{B.34}$$

B.2.1. Thermal design for the DC/AC converter with active power decoupling feature

The procedure for the thermal design of the DC/AC converter is the same as the one addressed in section B.1.1. The thermal design aims to find the thermal resistance $R_{\theta_{SA}}$ such that the junction temperature does not exceed $125°C$. The thermal parameters are shown in Table. B.6.

Table B.6. Parameters for the IGBT IXYP8N90C3D1 thermal design.

Parameter	**Symbol**	**Value**	**Units**
Dissipated power	P_D	13.22	W
Junction-case thermal resistance	$R_{\theta_{JC}}$	1.2	$°C/W$
Case-sink thermal resistance	$R_{\theta_{CS}}$	0.5	$°C/W$
Junction temperature	T_J	125	$°C$
Ambient temperature	T_J	40	$°C$

Considering the parameters in Table B.6, the sink-ambient thermal resistance is calculated as follows:

$$R_{\theta_{SA}} = \frac{T_J - T_A}{P_D} - R_{\theta_{JC}} - R_{\theta_{CS}} = 8.52°C/W. \tag{B.35}$$

Based on the thermal resistance obtained, a search and comparison of the different heatsink models were carried out in order to select the most suitable option for the raised thermal parameters. It was determined that EA-T220-64E heatsink from the manufacturer Ohmite was the best choice for the application addressed.

APPENDIX C

Design and implementation of the PCBs

In order to implement an experimental scenario for the converters evaluated in this work and validate their operation principle and performance, a PCB was designed and built for the Buck-Boost converter and the DC/AC converter with active power decoupling. In this appendix, the design considerations for the developed prototypes and the final results are shown.

C.1. PCB design and implementation for the Bidirectional Buck-Boost converter

The design of the Bidirectional Buck-Boost converter is based on the scheme presented in Chapter I. This converter has two IRFPS40N50L MOSFET switches (S_1 and S_2), including a heatsink PA-T2X-38E series for each one. The transfer inductor L is made of a ferrite core RM/14I type with 3C95 material. The decoupling capacitor Cz is formed by two BLH506K451B104 film capacitors connected in parallel to form a $100uF$ equivalent. The conditioning stage is made of two independent VO3120 drivers that provide optic isolation between the modulation stage and the power switching stage. These drivers are supplied by two isolated DC/DC converters (PDME1-S12-S12-S) that provide a regulated DC source. The power stage is comprised of the power MOSFETS, the transfer inductor and the arrangement of the film capacitors that represent de decoupling capacitor. In addition, some test points are incorporated for being to measure the parameters of interest on the PCB. The overall specifications of the Bidirectional Buck-Boost converter are shown in Table. C.1.

Table C.1. Overall components specifications of the Bidirectional Buck-Boost converter.

Parameter	**Symbol**	**Value**	**Units**	**Model**
Transfer inductor	L	620	μH	$RM14/I - RC95$
Decoupling capacitor	C_z	50	μF	BLH506K451B10
Power MOSFETs	S_1, S_2	–	–	IRFPS40N50L
Heatsinks	–	–	–	PA-T2X-38E
Isolated drivers	–	–	–	VO3120
Isolated DC/DC power supplies	–	–	–	PDME1-S12-S12-S
Final dimensions (width x length)	$w \times l$	20×20	cm	

Fig. C.1 shows the layout for the Bidirectional Buck-Boost converter.

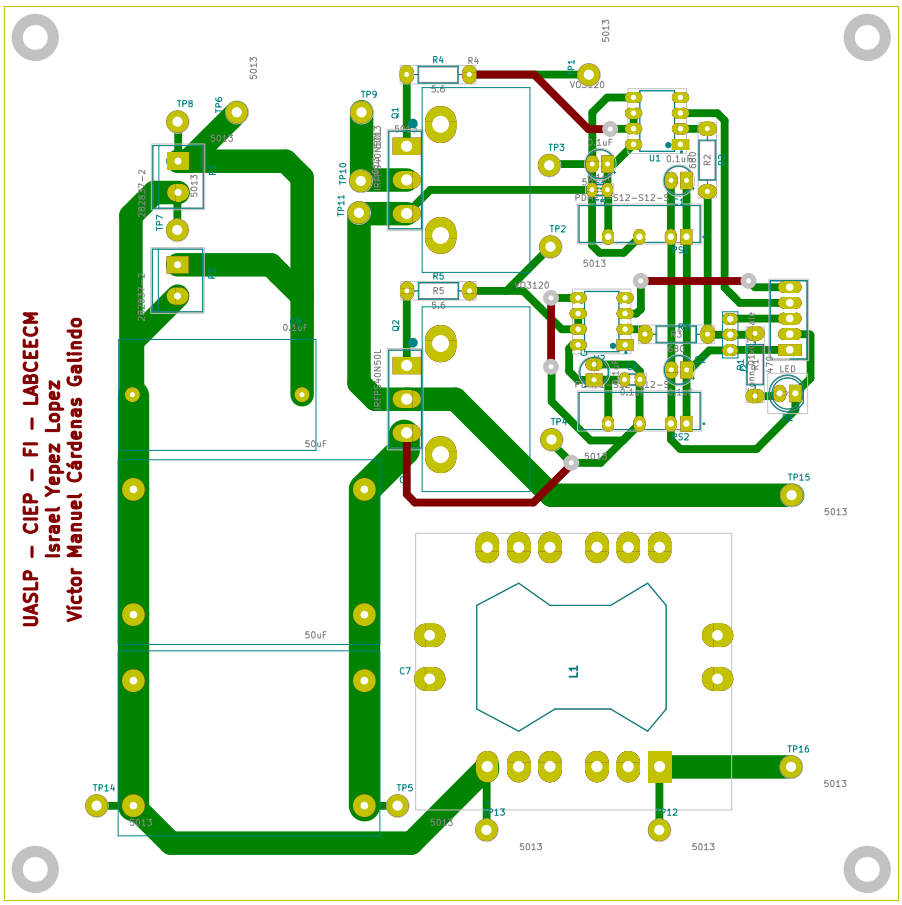


Figure C.1. Layout for the Bidirectional Buck-Boost converter.

The layout design consists of two layers: the back copper layer that includes the tracks in green and the front copper layer that is made up of the tracks in red. It can be seen that most of the tracks are in the back layer since at first the PCB was designed to have only one layer, however, it was necessary at the end to incorporate the front layer. This layout seeks to optimize the size as much as possible, as well as to properly position

and separate the digital and control stage from the power stage, this is made in order to avoid interference and noise on the digital stage. Trajectories were tracked as straight as possible to avoid unnecessary turns; in addition, it was considered to cross perpendicularly the tracks of the front layer with the back layer to avoid signal coupling. Finally, all the tracks were traced with the appropriate thickness considering the current that circulates through them.

Fig. C.2 shows the built PCB prototype with all the components such as the power MOSFETs, the film capacitor, the transfer inductor and the drivers. It should be noticed that there is a copper arc wire on the right of the transfer inductor to introduce the current measuring probe.

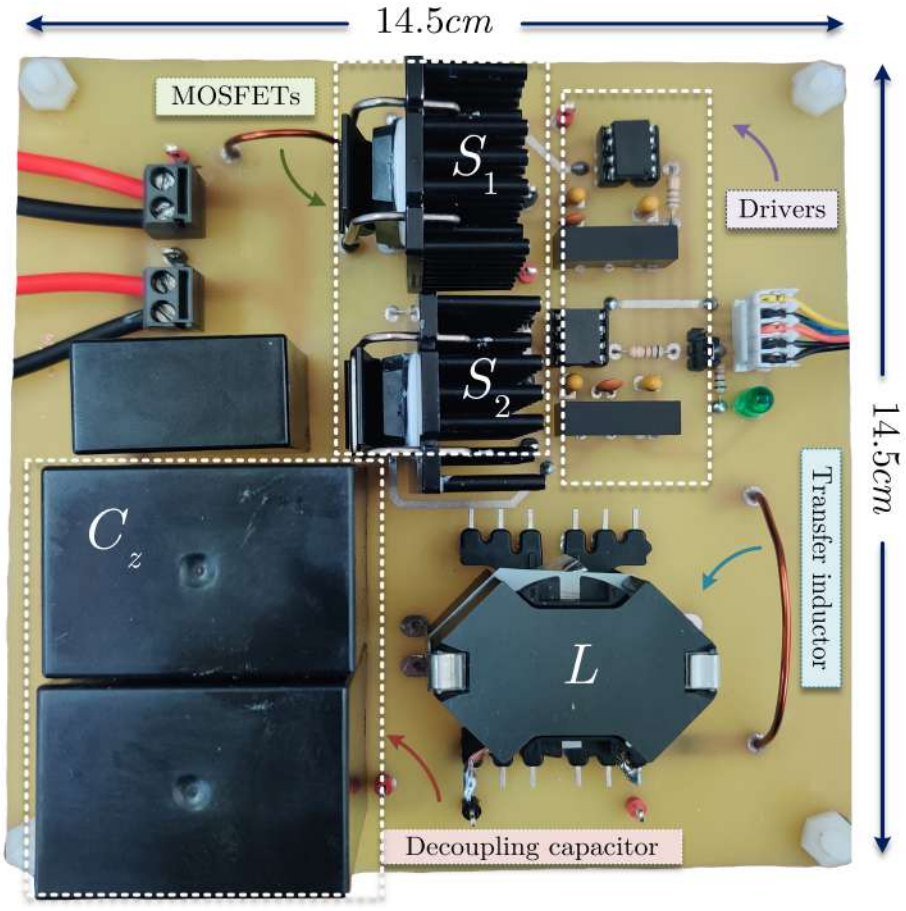
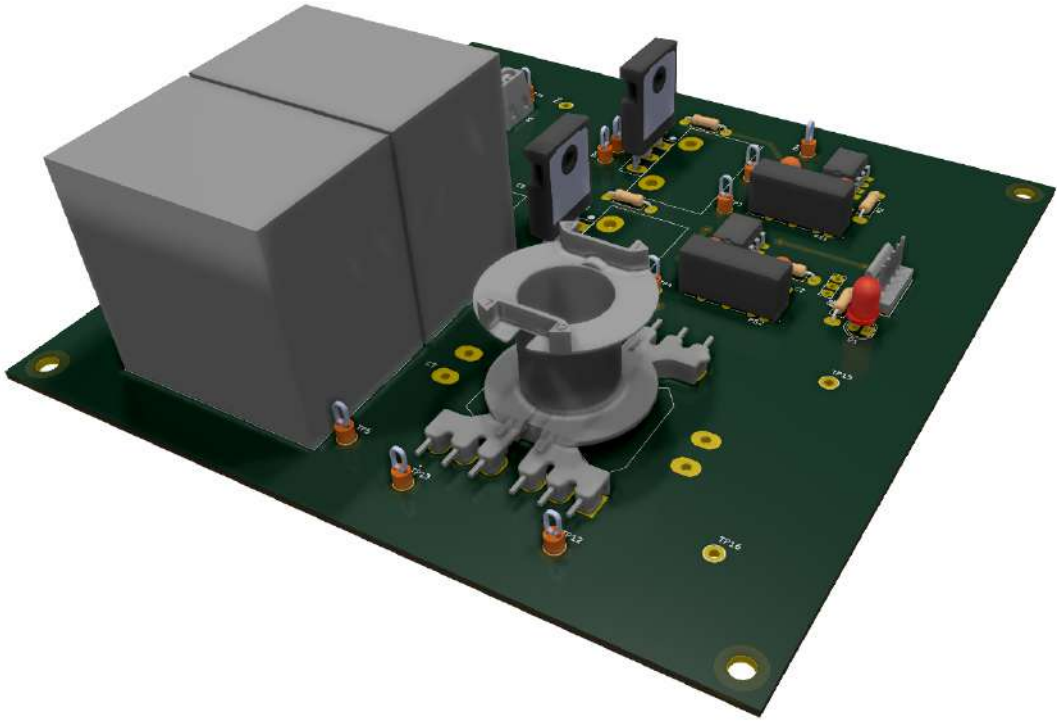


Figure C.2. Built Buck-Boost PCB prototype.

Finally, Fig. C.3 shows a comparison between the 3D PCB view and the final built prototype.



(a) 3D view.

(b) Built prototype.

Figure C.3. Comparison between the 3D PCB view and the final built Buck-Boost prototype.

C.2. PCB design and implementation for DC/AC converter with active power decoupling feature

The design of the DC/AC converter with active power decoupling is based on the scheme and the performance parameters defined in Chapter II. The converter has four IXYP8N90C3D1 IGBTs each including an EA-T220-64E model heatsink. The converter has two inductors (L_b) and (L_{inv}) made with an E-80/38/20 type ferrite core of N-87 material. The DC-link capacitor consists of a $30\mu F$ film capacitor with the part number BLH306K801B104. The LC filter capacitor is made up of a series arrangement of three $22\mu F$ capacitors with the part number B32524R3226J000 to form an equivalent capacitance of approximately $7.3\mu F$. The signal conditioning stage is made up of four TLP5772HLF4E drivers that provide optic isolation between the modulation stage and the power switching stage. These drivers are powered by isolated DC/DC converters (PDSE1-S12-S15-M) that provide a regulated and constant power supply; It should be noted that for the entire digital and conditioning stage, the use of SMD devices was used to optimize the size of the PCB. The power stage is composed of the IGBT switches ($S_1 - S_4$), the inductors L_b and L_{inv}, and the DC-link capacitor.

The overall specifications of the DC/AC converter with active power decoupling are shown in Table. C.2.

Table C.2. Overall components specifications of DC/AC converter.

Parameter	**Symbol**	**Value**	**Units**	**Model**
Boost inductor	L_b	1	μH	$E-80/38/20-N-87$
Inverter inductor	L_{inv}	1	μH	$E-80/38/20-N-87$
DC-link capacitor	C_{dc}	30	μF	BLH306K801B104
LC filter capacitor	C_{inv}	7.3	μF	B32524R3226J000
Power IGBTs	$S_1 - S_4$	–	–	IXYP8N90C3D1
Heatsinks	–	–	–	EA-T220-64E
Isolated drivers	–	–	–	TLP5772HLF4E
Isolated DC/DC power supplies	–	–	–	PDSE1-S12-S15-M
Final dimensions (width x length)	$w \times l$	20×20	cm	

Fig. C.4 shows the layout for the DC/AC converter with active power decoupling. The layout design consists of two layers: the back copper layer that includes the tracks in green and the front copper layer that is made up of the tracks in red.

In this PCB design, it was intended to homologate all the tracks of the power stage on the back copper layer (green tracks) while it was sought that all the tracks of the digital stage remain on the front cooper layer (red tracks) in such a way that it optimizes

the issue of isolation between the digital stage and conditioning of the power stage as much as possible. In addition, the driver stage is located close enough to the transistor to avoid the coupling of parasitic inductances preventing voltage overshoots on the switching signals. It was also sought to optimize the total size of the PCB, achieving a final size of approximately $20cm \times 20cm$; It should be noted that the converter includes an active power decoupling stage, a DC/CA conversion stage, the LC filter and the entire conditioning stage on the same PCB. Trajectories were tracked as straight as possible to avoid unnecessary turns; in addition, it was considered to cross perpendicularly the tracks of the front layer with the back layer to avoid signal coupling. Finally, all the tracks were traced with the appropriate thickness considering the current that circulates through them.

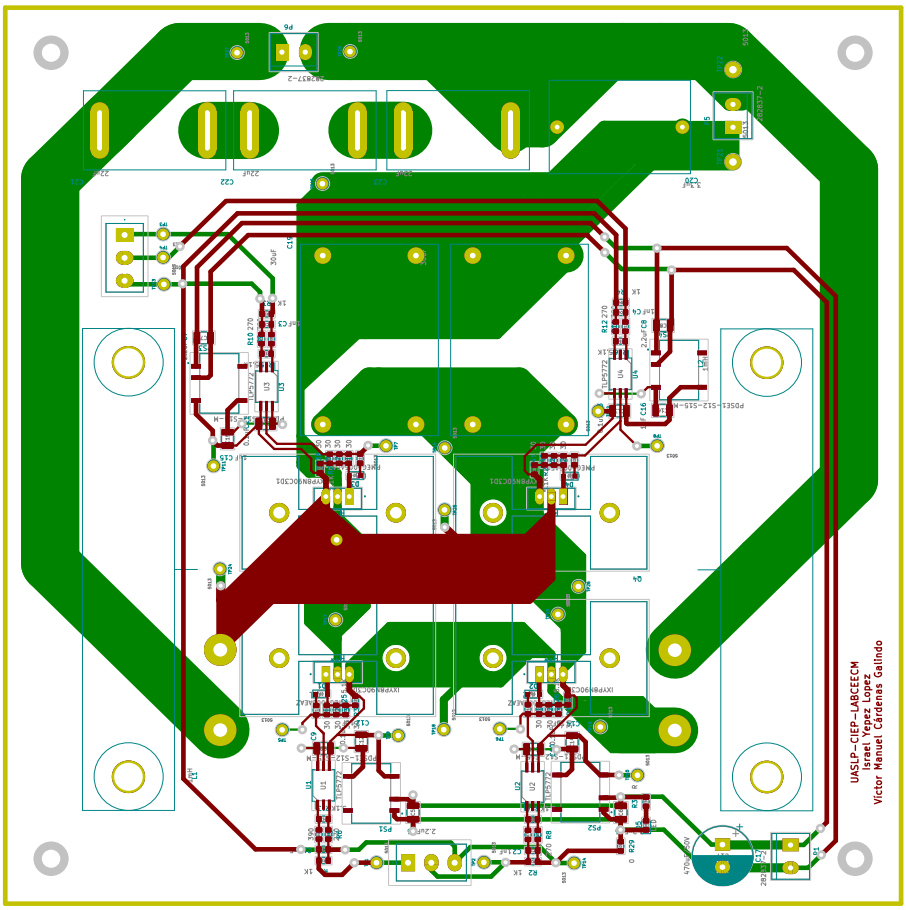


Figure C.4. Layout for the DC/AC converter.

Fig. C.5 shows the built PCB prototype with all the components such as the power IGBTSs, the DC-link capacitor, the transfer inductor, the LC filter inductor and capacitor and the drivers.

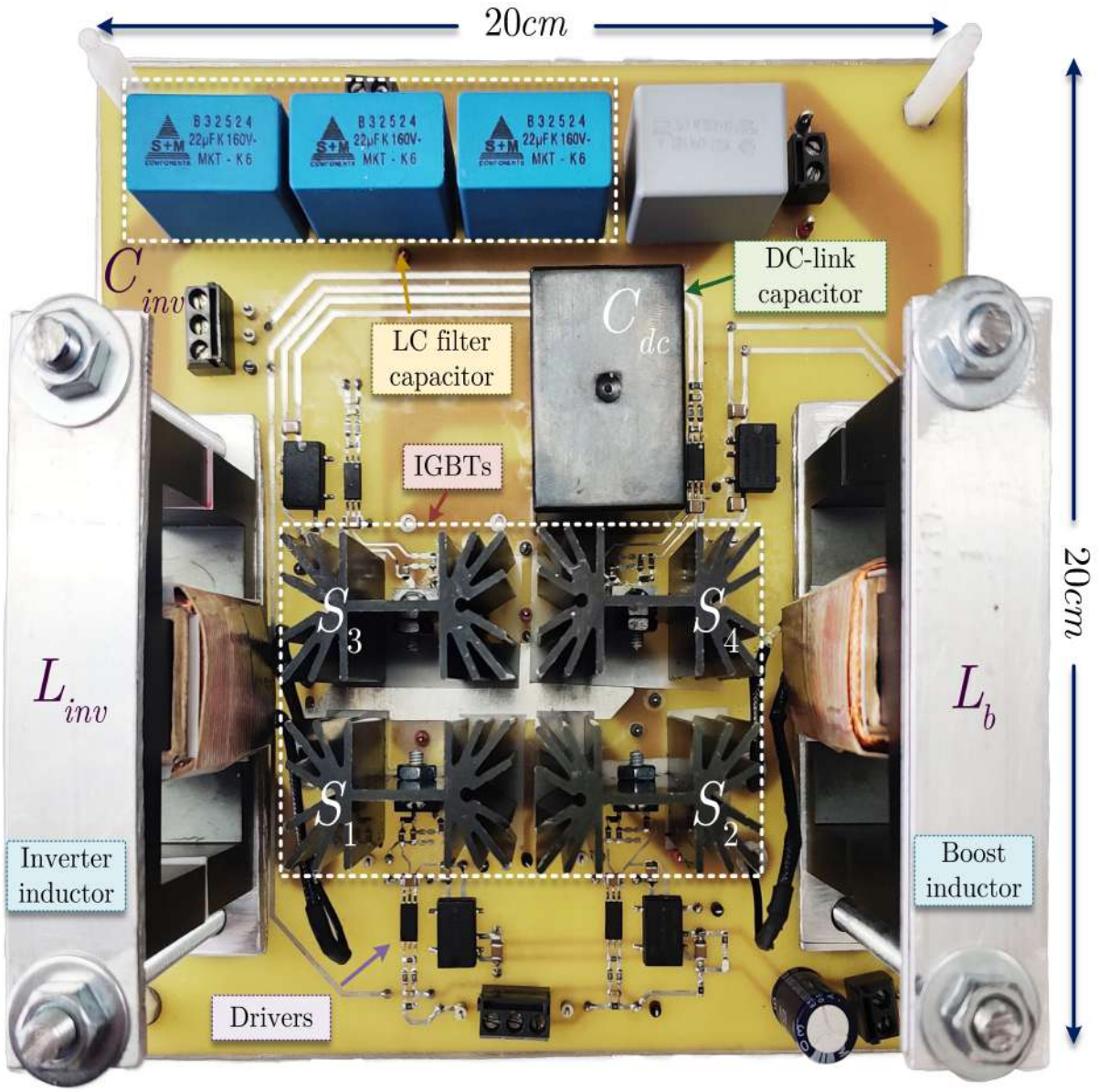
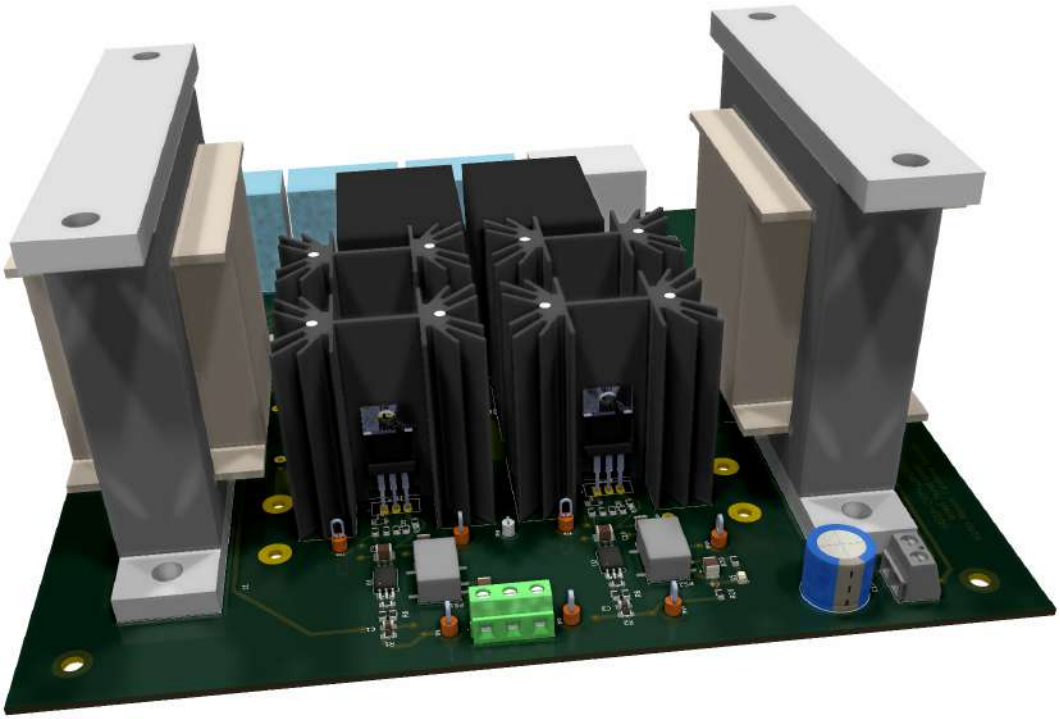
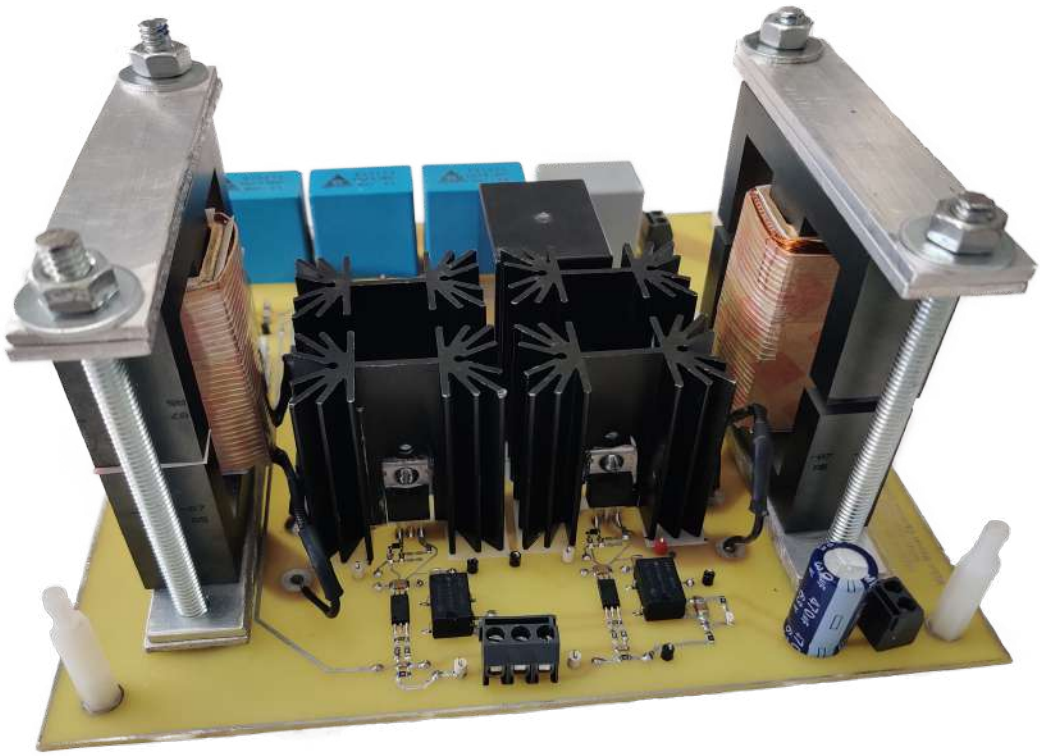


Figure C.5. Built DC/AC converter PCB prototype.

Finally, Fig. C.6 shows a comparison between the 3D PCB view and the final built prototype.



(a) 3D view.



(b) Built prototype.

Figure C.6. Comparison between the 3D PCB view and the final built DC/AC converter prototype.

References

[1] "Electricity information: Overview," tech. rep., International Energy Agency (IEA), 2021.

[2] "Renewable electricity," tech. rep., International Energy Agency (IEA), 2022.

[3] "Electricity sector," tech. rep., International Energy Agency (IEA), 2022.

[4] "Global energy review: Co2 emissions in 2021," tech. rep., International Energy Agency (IEA), 2022.

[5] "Renewables 2021 - analysis and forecast to 2026," tech. rep., International Energy Agency (IEA), 2021.

[6] "Prospectiva de energías renovables 2018 - 2032," tech. rep., Secretaría de energía (SENER), 2018.

[7] "Prospectiva del sector eléctrico 2018 - 2032," tech. rep., Secretaría de energía (SENER), 2018.

[8] "Ieee standard for interconnection and interoperability of distributed energy resources with associated electric power systems interfaces," *IEEE Std 1547-2018 (Revision of IEEE Std 1547-2003)*, pp. 1–138, 2018.

[9] S. Xu, M. Mao, R. Shao, and L. Chang, "Voltage-reference active power decoupling based on boost converter for single-phase bridge inverter," in *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, pp. 1793–1798, 2018.

[10] T. Sekiguchi and T. Shimizu, "Study on single-phase photovoltaic power generation system with power decoupling and generation control functions," in *2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia)*, pp. 1945–1951, 2019.

[11] V. Michal, "Switched-mode active decoupling capacitor allowing volume reduction of the high-voltage dc filters," *IEEE Transactions on Power Electronics*, vol. 31, no. 9, pp. 6104–6111, 2016.

[12] Y. Sun, Y. Liu, M. Su, W. Xiong, and J. Yang, "Review of active power decoupling topologies in single-phase systems," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 4778–4794, 2016.

[13] T. A. Pereira, D. C. Martins, and R. F. Coelho, "Active-capacitor for power decoupling in single-phase grid-connected converters," in *2019 IEEE 15th Brazilian Power Electronics Conference and 5th IEEE Southern Power Electronics Conference (COBEP/SPEC)*, pp. 1–6, 2019.

[14] J.-i. Itoh, T. Sakuraba, K. Kusaka, H. Watanabe, and K. Furukawa, "Comparison of circuit topologies for active power decoupling toward high power density," in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, pp. 421–428, 2016.

[15] A. Aganza, "Desarrollo de un convertidor matricial monofásico con enlace en alta frecuencia para sistemas fotovoltaicos en microgeneración eléctrica," 2012.

[16] G. Kafanas, M. R. Jeffrey, and X. Yuan, "Variable structure control for active power decoupling topologies," in *8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016)*, pp. 1–6, 2016.

[17] S. Xu, L. Chang, and R. Shao, "Evolution of single-phase power converter topologies underlining power decoupling," *Chinese Journal of Electrical Engineering*, vol. 2, no. 1, pp. 24–39, 2016.

[18] Z. Qin, Y. Tang, P. C. Loh, and F. Blaabjerg, "Benchmark of ac and dc active power decoupling circuits for second-order harmonic mitigation in kilowatt-scale single-phase inverters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 1, pp. 15–25, 2016.

[19] R. Wang, F. Wang, D. Boroyevich, and P. Ning, "A high power density single phase pwm rectifier with active ripple energy storage," in *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1378–1383, 2010.

[20] B. Koushki, P. Jain, and A. Bakhshai, "Minimum conduction loss zvs control for buck-type active filter operating as decoupling circuit," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1322–1328, 2018.

[21] B. Ge, X. Li, H. Zhang, Y. Liu, R. S. Balog, H. Abu-Rub, and L. Alpuerto, "Direct instantaneous ripple power predictive control for active ripple decoupling of single-

phase inverter," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 4, pp. 3165–3175, 2018.

[22] J. Hong, M. Vilathgamuwa, J. Yin, Y. Liu, J. Peng, and H. Jiang, "Power decoupling of a single phase dc-ac dual active bridge converter based on an integrated bidirectional buck/boost stage," *Energies*, vol. 11, no. 10, 2018.

[23] Z. Lin, M. Su, Y. Liu, Y. Sun, Y. Liao, and X. Chen, "Single-phase integrated power decoupling inverter based on boost converter," in *2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia)*, pp. 405–408, 2020.

[24] Y. Xia, J. Roy, and R. Ayyanar, "A capacitance-minimized, doubly grounded transformer less photovoltaic inverter with inherent active-power decoupling," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5188–5201, 2017.

[25] H. Zhao, H. Li, C. Min, and K. Zhang, "A modified single-phase h-bridge pwm rectifier with power decoupling," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, pp. 80–85, 2012.

[26] S. A. Sabeeh Al-Obaidi, K. C. Hodge, and P. Enjeti, "A dual-phase output 4-leg inverter with active decoupling and integrated power optimizer for off-grid applications," in *2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, pp. 1–6, 2018.

[27] Y. Tang and F. Blaabjerg, "A component-minimized single-phase active power decoupling circuit with reduced current stress to semiconductor switches," *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 2905–2910, 2015.

[28] D.-H. Hwang, J.-Y. Lee, and Y. Cho, "Pcc voltage compensation of pv inverter with active power decoupling circuit," in *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, pp. 1403–1408, 2018.

[29] M. Su, P. Pan, X. Long, Y. Sun, and J. Yang, "An active power-decoupling method for single-phase ac–dc converters," *IEEE Transactions on Industrial Informatics*, vol. 10, no. 1, pp. 461–468, 2014.

[30] B. Liu, Z. Zhang, G. Li, D. He, Y. Chen, Z. Zhang, G. Li, and S. Song, "Integration of power decoupling buffer and grid-tied photovoltaic inverter with single-inductor dual-buck topology and single-loop direct input current ripple control method,"

International Journal of Electrical Power & Energy Systems, vol. 125, p. 106423, 2021.

[31] S. Xiao, X. Li, H. Zhang, and R. S. Balog, "Active power decoupling method based on dual buck circuit with model predictive control," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 3089–3094, 2018.

[32] D.-H. Hwang, J.-Y. Lee, and Y. Cho, "Single-phase single-stage dual-buck photovoltaic inverter with active power decoupling strategy," *Renewable Energy*, vol. 126, pp. 454–464, 2018.

[33] F. Schimpf and L. Norum, "Effective use of film capacitors in single-phase pv-inverters by active power decoupling," in *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, pp. 2784–2789, 2010.

[34] A. Aganza-Torres, V. Cárdenas, H. Miranda-Vidales, and J. Alcalá, "Decoupling capacitor minimization in hf-link single-phase cycloconverter based microinverter," *Solar Energy*, vol. 105, pp. 590–602, 2014.

[35] T. Shimizu and S. Suzuki, "A single-phase grid-connected inverter with power decoupling function," in *The 2010 International Power Electronics Conference - ECCE ASIA -*, pp. 2918–2923, 2010.

[36] H. Watanabe, K. Kusaka, K. Furukawa, K. Orikawa, and J.-i. Itoh, "Dc to single-phase ac voltage source inverter with power decoupling circuit based on flying capacitor topology for pv system," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1336–1343, 2016.

[37] M. Qiu, P. Wang, H. Bi, and Z. Wang, "Active power decoupling design of ac-dc converter for on-board chargers," in *2019 22nd International Conference on Electrical Machines and Systems (ICEMS)*, pp. 1–5, 2019.

[38] Q.-C. Zhong, W.-L. Ming, X. Cao, and M. Krstic, "Control of ripple eliminators to improve the power quality of dc systems and reduce the usage of electrolytic capacitors," *IEEE Access*, vol. 4, pp. 2177–2187, 2016.

[39] X. Cao, Q.-C. Zhong, and W.-L. Ming, "Ripple eliminator to smooth dc-bus voltage and reduce the total capacitance required," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 4, pp. 2224–2235, 2015.

[40] M. Qiu, P. Wang, H. Bi, and Z. Wang, "Active power decoupling design of a single-phase ac–dc converter," *Electronics*, vol. 8, no. 8, 2019.

[41] L. Nicieza, "Dc-link cancellation in single phase converters," 2017.

[42] D. Z. Gao and K. Sun, "16 - dc–ac inverters," in *Electric Renewable Energy Systems* (M. H. Rashid, ed.), pp. 354–381, Boston: Academic Press, 2016.

[43] F. Quiroz, "Desarrollo de un inversor fotovoltaico con funciones autónomas para generación eléctrica distribuida," 2019.

[44] N. Mohan, W. Robbins, P. Imbertson, T. Undeland, R. Panaitescu, A. Jain, P. Jose, and T. Begalke, "Restructuring of first courses in power electronics and electric drives that integrates digital control," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 429–437, 2003.

[45] R. Teodorescu, M. Liserre, and P. Rodriguez, *Grid Synchronization in SinglePhase Power Converters*, pp. 43–91. 2007.

[46] M. González, "Estudio de la tranformación dq para el cálculo de potencia activa y reactiva en filtros activos de corriente para cancelación armónica.," 2004.

[47] J. González, "Desarrollo e implementación de una microrred aislada con generación fotovoltaica.," 2020.

[48] J. Alcalá. 2016.

[49] C. McLyman, *Transformer and Inductor Design Handbook*. CRC Press, 2017.

[50] TOSHIBA, "Power mosfet electrical characteristics," tech. rep., Toshiba Electronic Devices and Storage Corporation, 2018.

[51] Infineon, "Mosfet power losses calculation using the datasheet parameters," tech. rep., Infineon Technologies AG, 2016.

[52] STMicroelectronics, "Calculation of conduction losses in a power rectifier," tech. rep., STMicroelectronics, 2011.

[53] I. Rectifier, "The hexfred ultrafast diode in power switching circuits," tech. rep., International Rectifier, 1992.

[54] T. Instruments, "Estimating mosfet parameters from the data sheet," tech. rep., Texas Instruments, 2002.

[55] POWEREX, "Igbt application notes powerex," tech. rep., POWEREX, 2005.

[56] M. ELECTRIC, "Igbt modules application note," tech. rep., MITSUBISHI ELECTRIC, 2014.